

Digitális Integrált Áramkörök katalóguslapjai

segédlet a Digitális Technika tantárgy
laboratóriumi gyakorlataihoz

(harmadik, átdolgozott változat)

A Texas Instruments adatlapjai
alapján összeállította:

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AUTOMATIKA INTÉZET

2003

| |
|---|
| <p>Figyelem! Néhány adatlapon a jobb áttekinthetőség érdekében bizonyos átszerkesztéseket hajtottunk végre, ezek azonban a tényszerűséget nem befolyásolják.</p> |
|---|

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SN5400, SN54LS00, SN54S00 SN7400, SN74LS00, SN74S00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

SDLS025 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

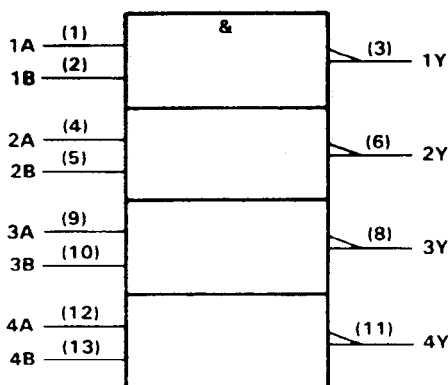
These devices contain four independent 2-input-NAND gates.

The SN5400, SN54LS00, and SN54S00 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7400, SN74LS00, and SN74S00 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

logic symbol†

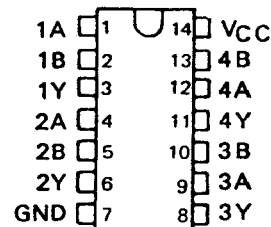


† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

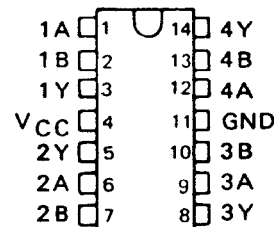
SN5400 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400 . . . N PACKAGE
SN74LS00, SN74S00 . . . D OR N PACKAGE

(TOP VIEW)



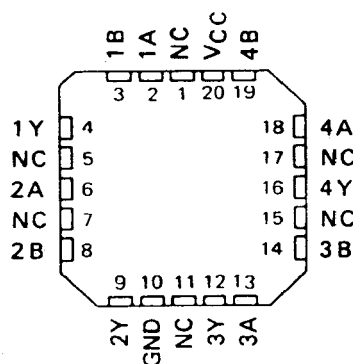
SN5400 . . . W PACKAGE

(TOP VIEW)



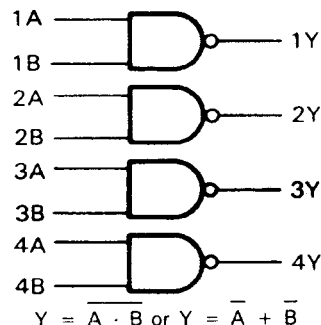
SN54LS00, SN54S00 . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A} + \overline{B}$$

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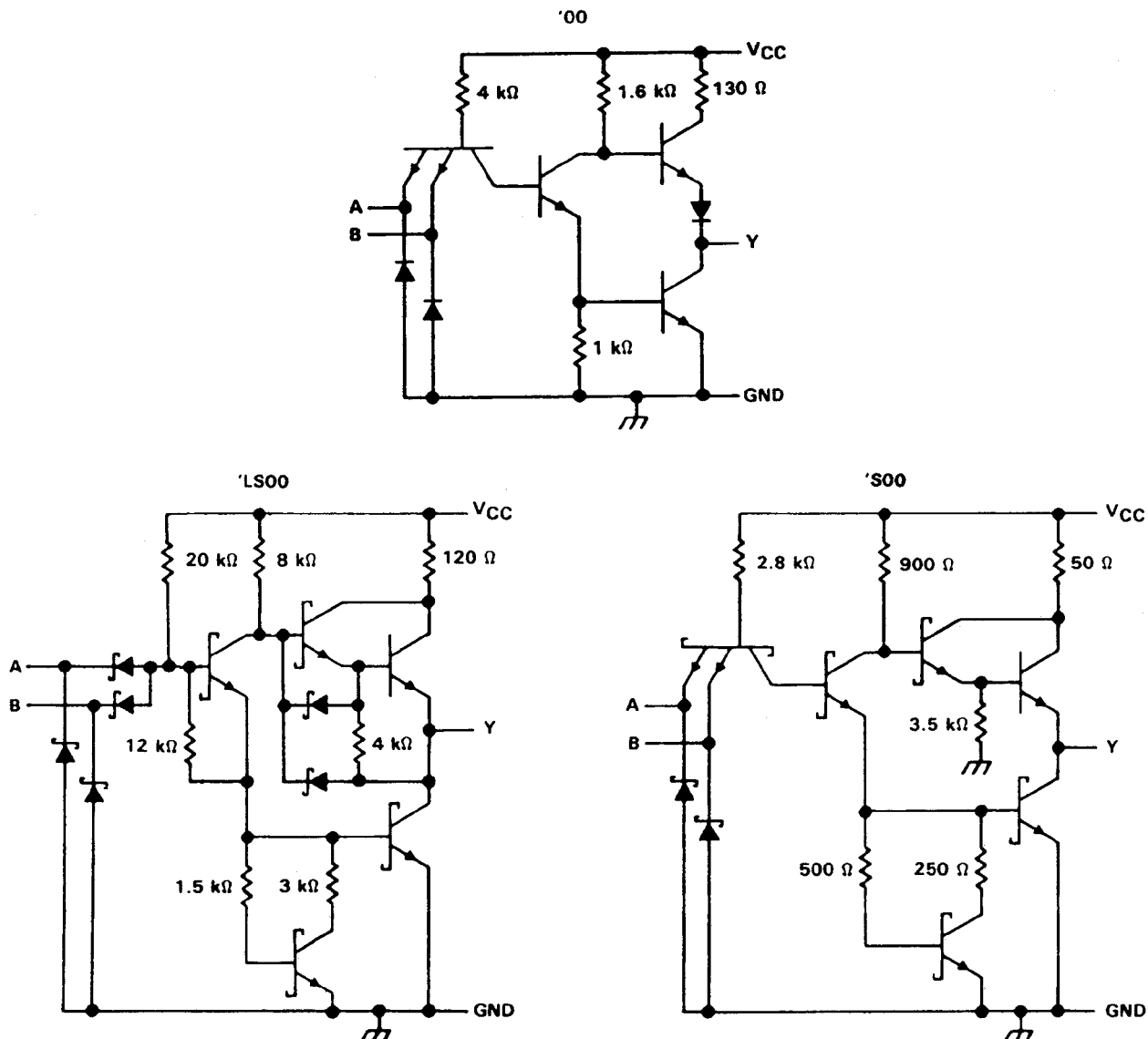
**TEXAS
INSTRUMENTS**

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SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES
SDLS025 – DECEMBER 1983 – REVISED MARCH 1988

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: '00, 'S00 | 5.5 V |
| 'LS00 | 7 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.



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SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00
QUADRUPL 2-INPUT POSITIVE-NAND GATES
SDLS025 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

| | SN5400 | | | SN7400 | | | UNIT |
|---|--------|-----|-------|--------|-----|-------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} High-level output current | | | – 0.4 | | | – 0.4 | mA |
| I _{OL} Low-level output current | | | 16 | | | 16 | mA |
| T _A Operating free-air temperature | – 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS † | SN5400 | | | SN7400 | | | UNIT |
|-------------------|--|--------|-------|-------|--------|-------|-------|------|
| | | MIN | TYP ‡ | MAX | MIN | TYP ‡ | MAX | |
| V _{IK} | V _{CC} = MIN, I _I = – 12 mA | | | – 1.5 | | | – 1.5 | V |
| V _{OH} | V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = – 0.4 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| I _I | V _{CC} = MAX, V _I = 5.5 V | | | 1 | | | 1 | mA |
| I _{IH} | V _{CC} = MAX, V _I = 2.4 V | | | 40 | | | 40 | µA |
| I _{IL} | V _{CC} = MAX, V _I = 0.4 V | | | – 1.6 | | | – 1.6 | mA |
| I _{OS} § | V _{CC} = MAX | – 20 | | – 55 | – 18 | | – 55 | mA |
| I _{CCH} | V _{CC} = MAX, V _I = 0 V | | 4 | 8 | | 4 | 8 | mA |
| I _{CCL} | V _{CC} = MAX, V _I = 4.5 V | | 12 | 22 | | 12 | 22 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--------------|-------------|--|-----|-----|-----|------|
| t _{PLH} | A or B | Y | R _L = 400 Ω, C _L = 15 pF | | 11 | 22 | ns |
| t _{PHL} | | | | | 7 | 15 | ns |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES
SDLS025 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

| | SN54LS00 | | | SN74LS00 | | | UNIT |
|---|----------|-----|-------|----------|-----|-------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.7 | | | 0.8 | V |
| I _{OH} High-level output current | | | – 0.4 | | | – 0.4 | mA |
| I _{OL} Low-level output current | | | 4 | | | 8 | mA |
| T _A Operating free-air temperature | – 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS † | SN54LS00 | | | SN74LS00 | | | UNIT |
|-------------------|--|----------|-------|-------|----------|-------|-------|------|
| | | MIN | TYP ‡ | MAX | MIN | TYP ‡ | MAX | |
| V _{IK} | V _{CC} = MIN, I _I = – 18 mA | | | – 1.5 | | | – 1.5 | V |
| V _{OH} | V _{CC} = MIN, V _{IL} = MAX, I _{OH} = – 0.4 mA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 8 mA | | | | | 0.35 | 0.5 | |
| I _I | V _{CC} = MAX, V _I = 7 V | | | 0.1 | | | 0.1 | mA |
| I _{IH} | V _{CC} = MAX, V _I = 2.7 V | | | 20 | | | 20 | µA |
| I _{IL} | V _{CC} = MAX, V _I = 0.4 V | | | – 0.4 | | | – 0.4 | mA |
| I _{OS} § | V _{CC} = MAX | – 20 | | – 100 | – 20 | | – 100 | mA |
| I _{CCH} | V _{CC} = MAX, V _I = 0 V | | 0.8 | 1.6 | | 0.8 | 1.6 | mA |
| I _{CCL} | V _{CC} = MAX, V _I = 4.5 V | | 2.4 | 4.4 | | 2.4 | 4.4 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|-----------------|----------------|---|-----|-----|-----|------|
| t _{PLH} | A or B | Y | R _L = 2 kΩ, C _L = 15 pF | | 9 | 15 | ns |
| t _{PHL} | | | | | 10 | 15 | ns |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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SN5402, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

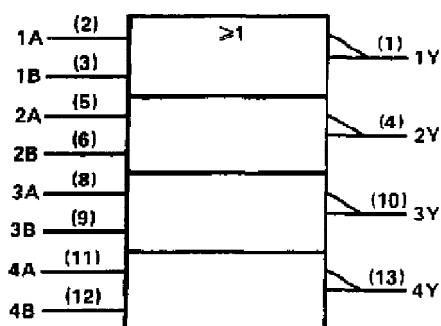
These devices contain four independent 2-input-NOR gates.

The SN5402, SN54LS02, and SN54S02 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7402, SN74LS02, and SN74S02 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | L |
| X | H | L |
| L | L | H |

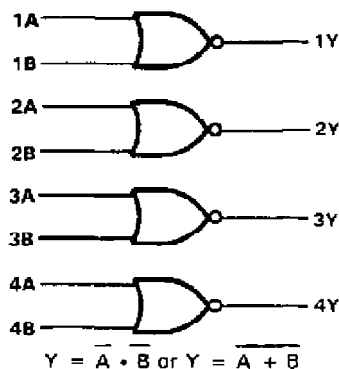
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

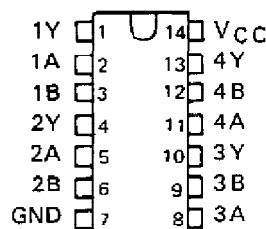
logic diagram (positive logic)



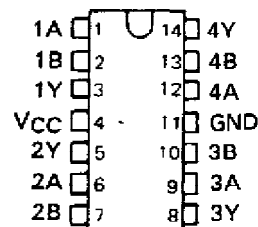
$$Y = A \cdot B \text{ or } Y = A + B$$

SN5402 . . . J PACKAGE
SN54LS02, SN54S02 . . . J OR W PACKAGE
SN7402 . . . N PACKAGE
SN74LS02, SN74S02 . . . D OR N PACKAGE

(TOP VIEW)

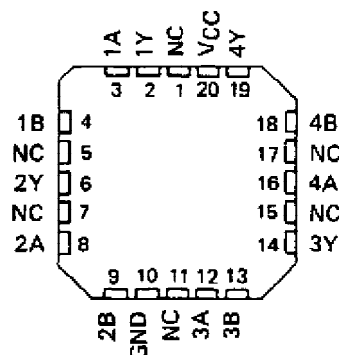


SN5402 . . . W PACKAGE
(TOP VIEW)



SN54LS02, SN54S02 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

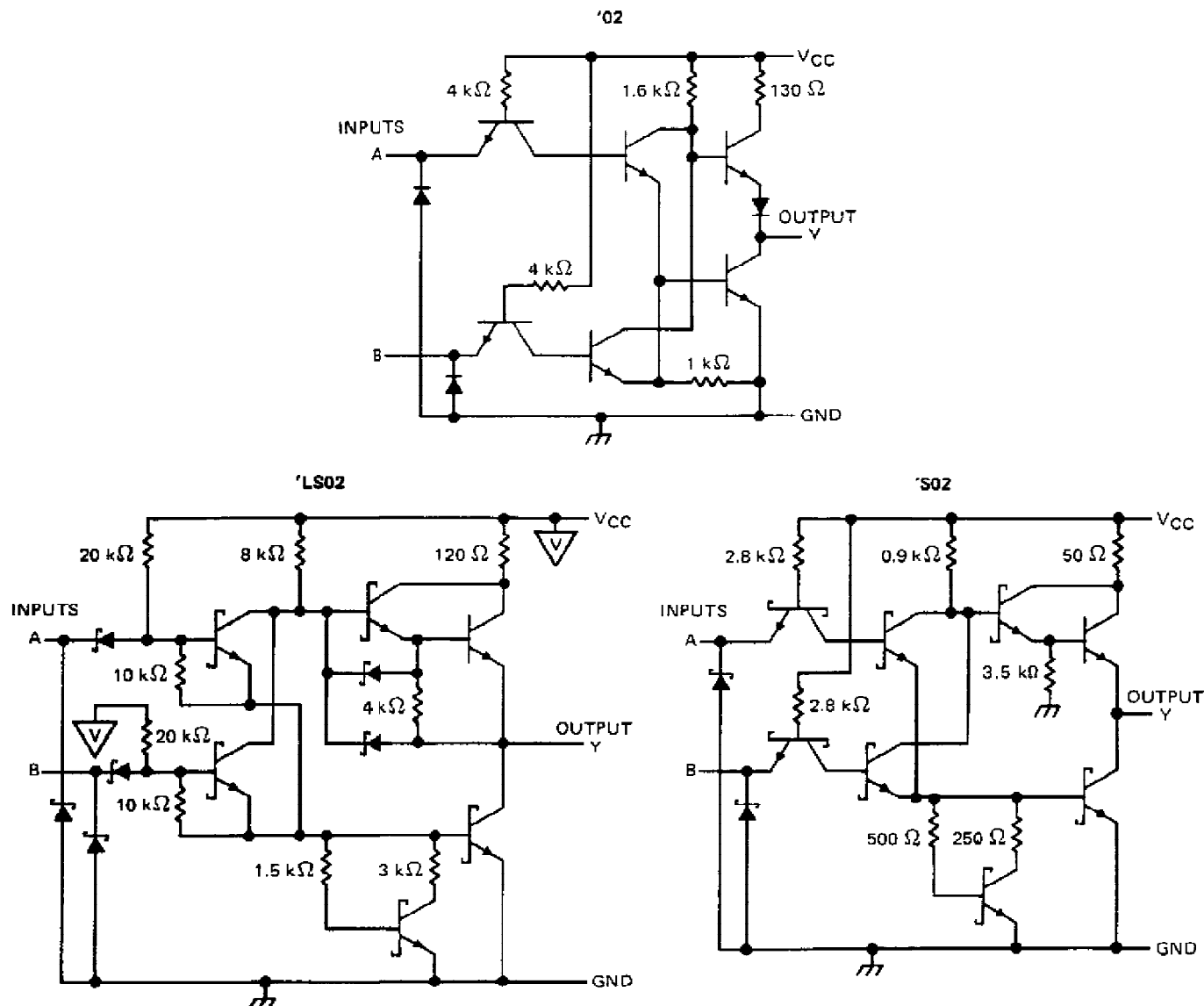
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SN5402, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02 **QUADRUPLE 2-INPUT POSITIVE-NOR GATES**

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: '02, 'S02 | 5.5 V |
| 'LS02 | 7 V |
| Off-state output voltage | 7 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1. Voltage values are with respect to network ground terminal.

**TEXAS
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QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

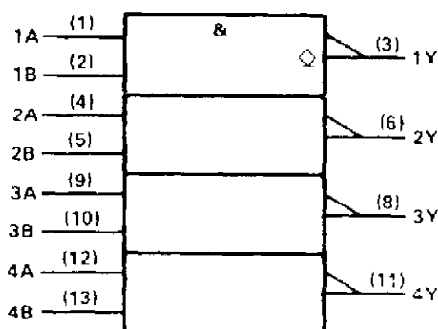
These devices contain four independent 2-input-NAND gates. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN5403, SN54LS03 and SN54S03 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7403, SN74LS03 and SN74S03 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

logic symbol†

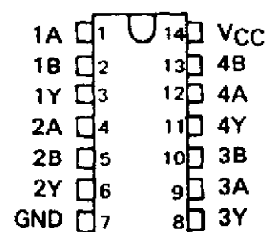


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

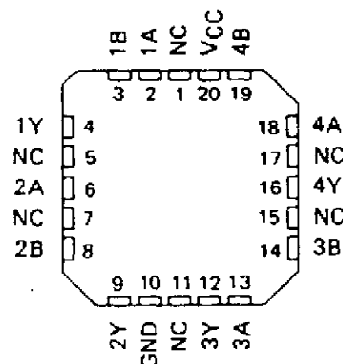
SN5403 . . . J OR W PACKAGE
 SN54LS03, SN54S03 . . . J OR W PACKAGE
 SN7403 . . . N PACKAGE
 SN74LS03, SN74S03 . . . D OR N PACKAGE

(TOP VIEW)



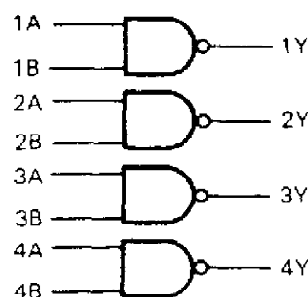
SN54LS03, SN54S03 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

logic diagram (positive logic)



$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A + B}$$

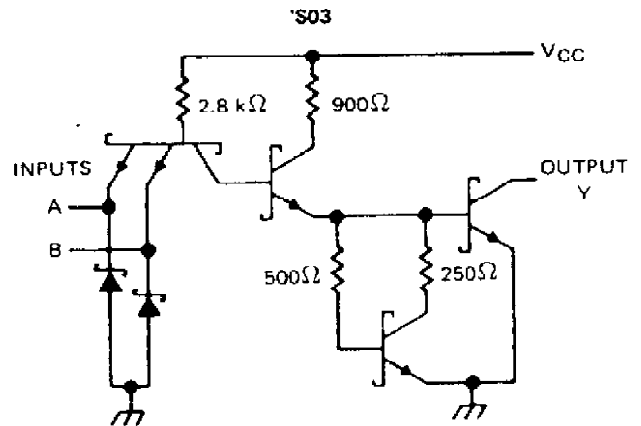
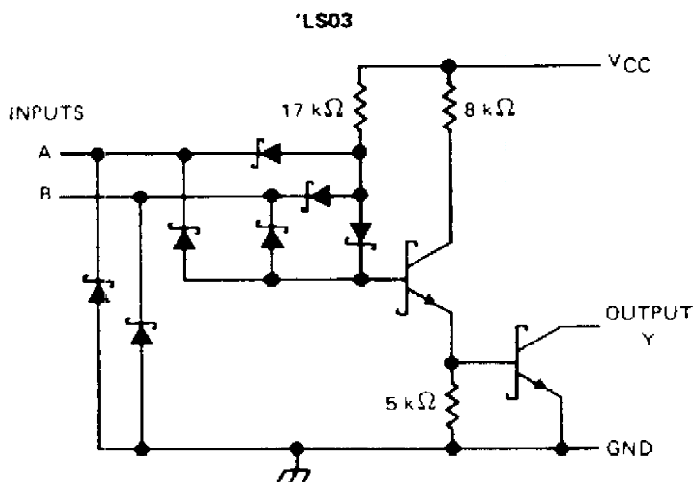
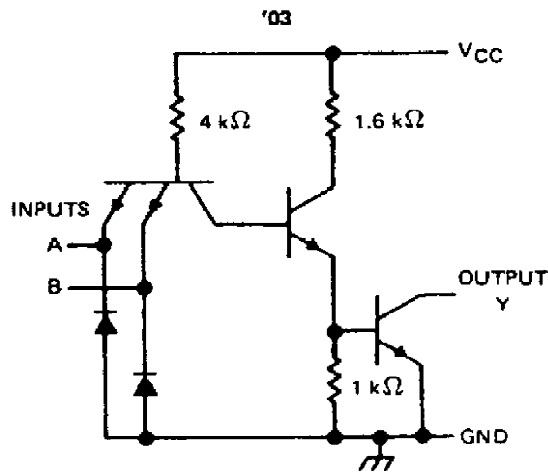
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TEXAS
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**SN5403, SN54LS03, SN54S03,
SN7403, SN74LS03, SN74S03**
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: '03, 'S03 | 5.5 V |
| 'LS03 | 7 V |
| Off-state output voltage | 7 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SN5404, SN54LS04, SN54S04, SN7404, SN74LS04, SN74S04 HEX INVERTERS

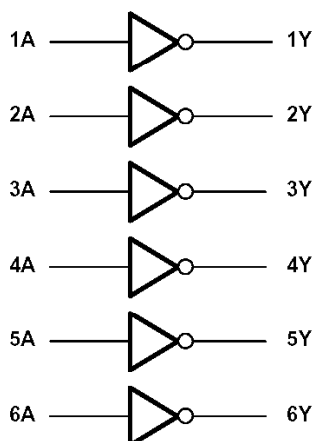
SDLS029B – DECEMBER 1983 – REVISED FEBRUARY 2002

- Dependable Texas Instruments Quality and Reliability

description

These devices contain six independent inverters.

logic diagram (positive logic)



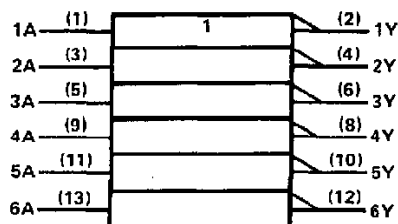
$$Y = \bar{A}$$

Pin numbers shown are for the D, DB, J, N, NS, and W packages.

FUNCTION TABLE
(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

logic symbol†

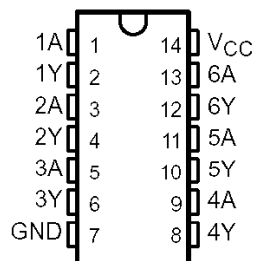


†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

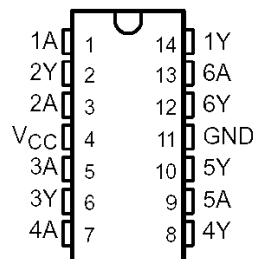
Pin numbers shown are for D, J, and N packages.

SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
SN74S04 . . . D OR N PACKAGE

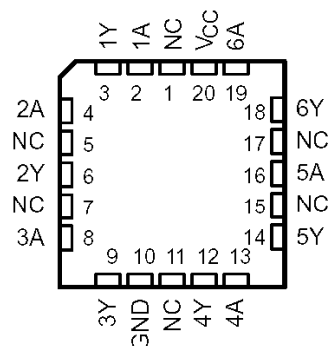
(TOP VIEW)



SN5404 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

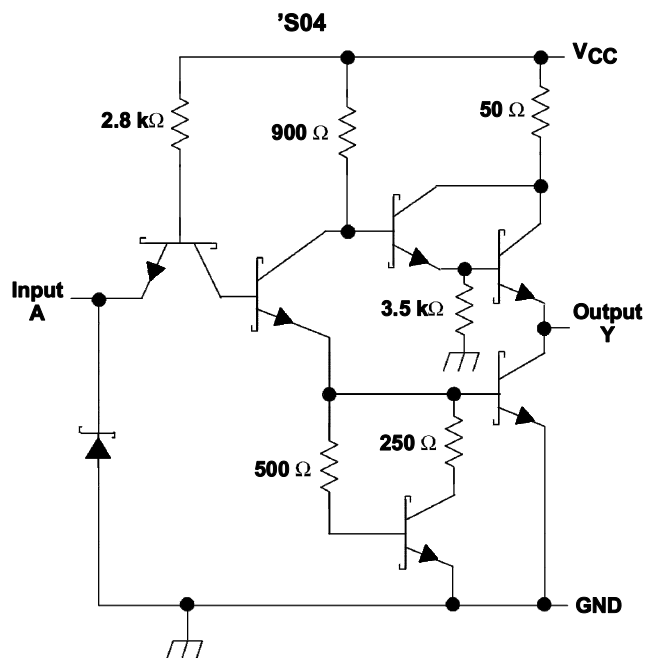
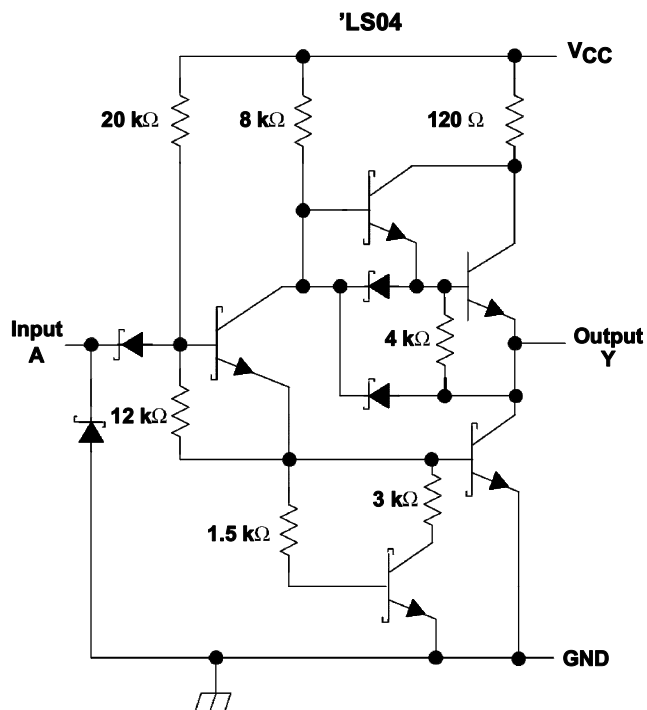
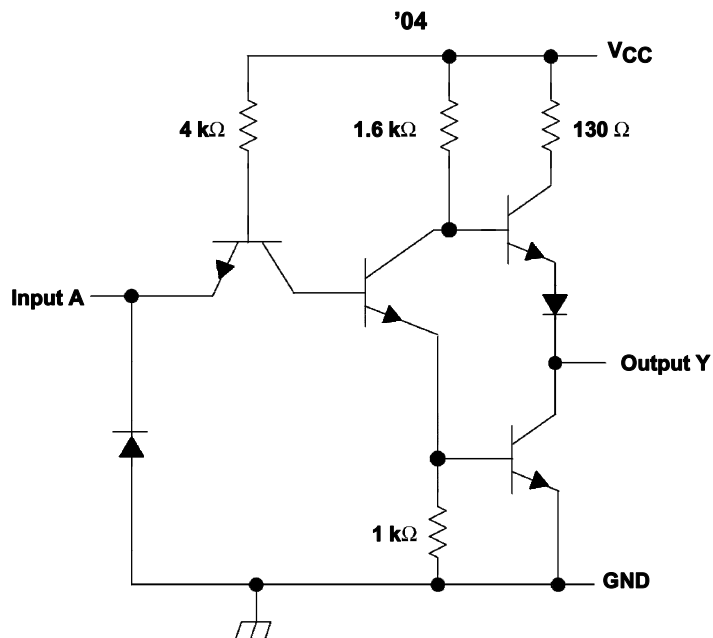
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN5404, SN54LS04, SN54S04, SN7404, SN74LS04, SN74S04 HEX INVERTERS

SDLS029B – DECEMBER 1983 – REVISED FEBRUARY 2002

schematics (each gate)



Resistor values shown are nominal.

SN5408, SN54LS08, SN54S08 SN7408, SN74LS08, SN74S08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

SDLS033—DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

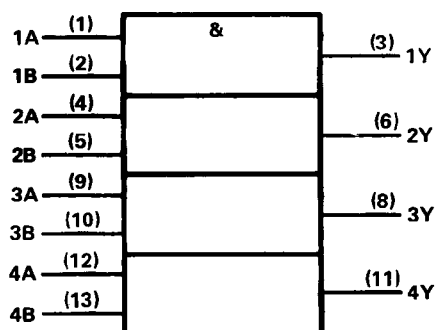
These devices contain four independent 2-input AND gates.

The SN5408, SN54LS08, and SN54S08 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7408, SN74LS08 and SN74S08 are characterized for operation from 0° to 70°C .

FUNCTION TABLE (each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

logic symbol†

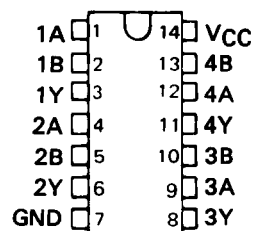


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

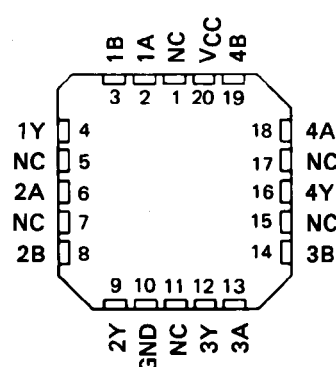
SN5408, SN54LS08, SN54S08 . . . J OR W PACKAGE
SN7408 . . . J OR N PACKAGE
SN74LS08, SN74S08 . . . D, J OR N PACKAGE

(TOP VIEW)



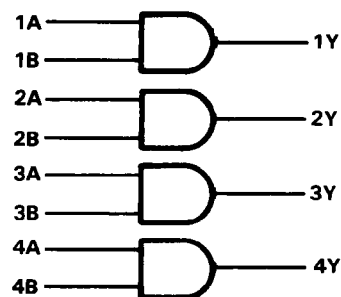
SN54LS08, SN54S08 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



$$Y = A \cdot B \text{ or } Y = \overline{\overline{A} + \overline{B}}$$

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TEXAS
INSTRUMENTS

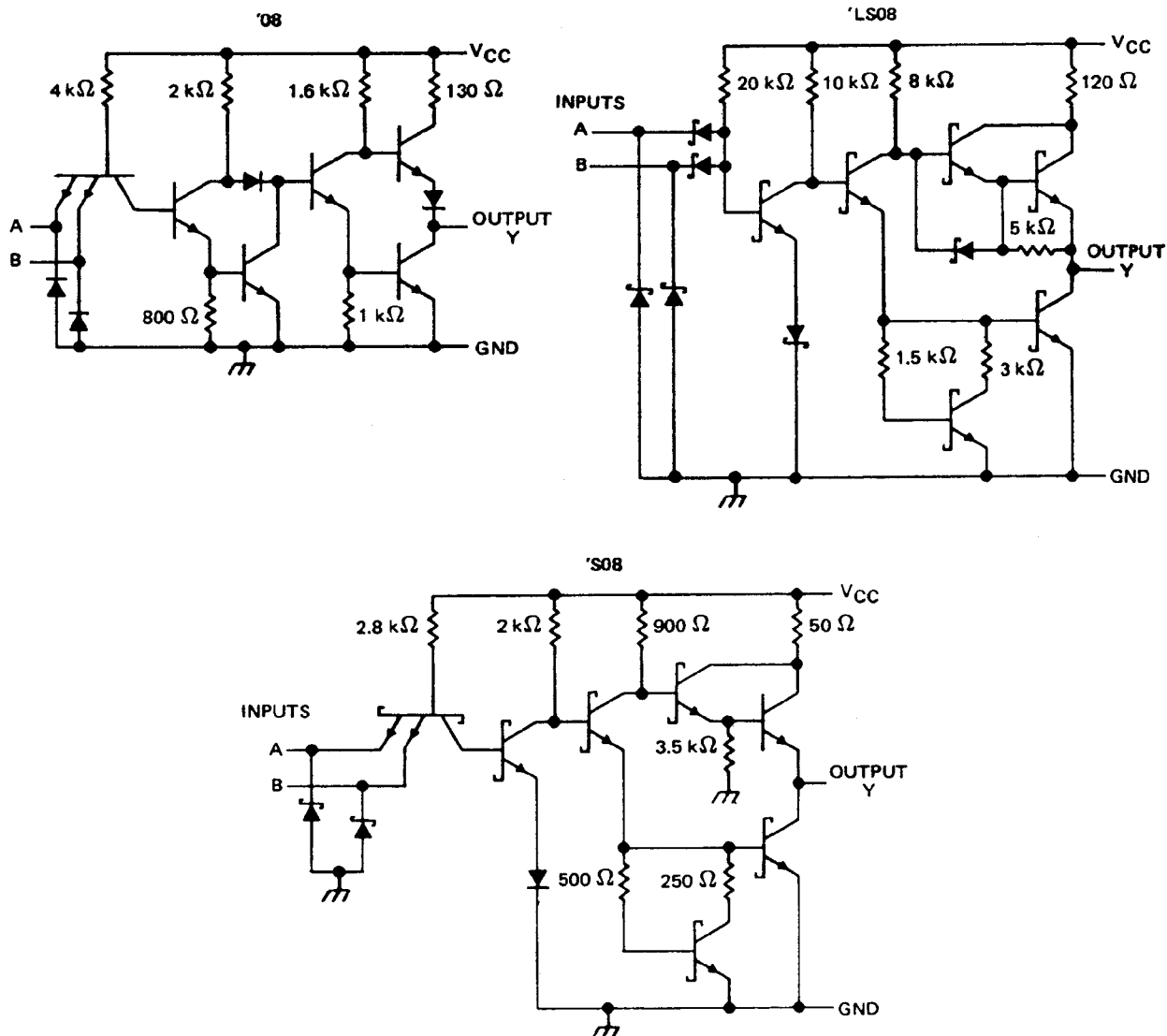
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SN5408, SN54LS08, SN54S08 SN7408, SN74LS08, SN74S08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

SDLS033—DECEMBER 1983—REVISED MARCH 1988

schematics (each gate)



Resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: '08, 'S08 | 5.5 V |
| 'LS08 | 7 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN5414, SN54LS14, SN7414, SN74LS14 HEX SCHMITT-TRIGGER INVERTERS

SDLS049B – DECEMBER 1983 – REVISED FEBRUARY 2002

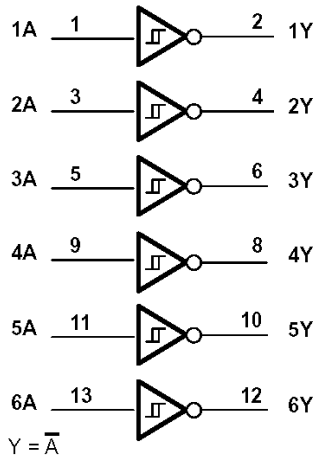
- Operation From Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

description

Each circuit functions as an inverter, but because of the Schmitt action, it has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

logic diagram (positive logic)

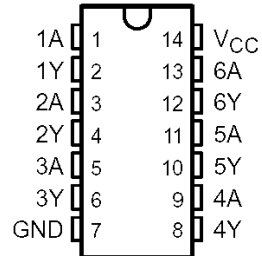


Pin numbers shown are for the D, DB, J, N, NS, and W packages.

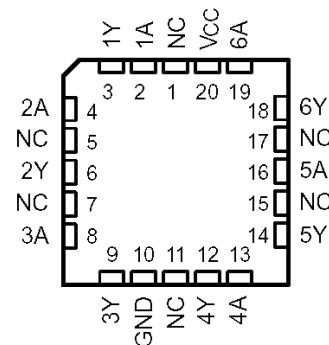
FUNCTION TABLE
(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

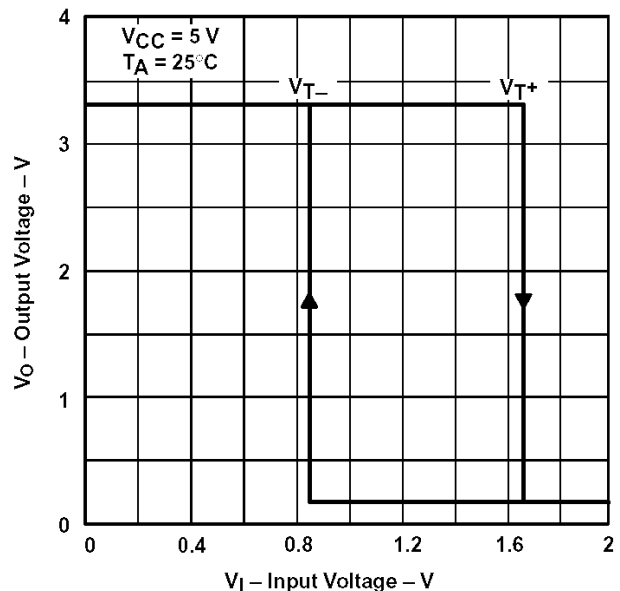
SN5414, SN54LS14 ... J OR W PACKAGE
SN7414 ... D, N, OR NS PACKAGE
SN74LS14 ... D, DB, OR N PACKAGE
(TOP VIEW)



SN54LS14 ... FK PACKAGE
(TOP VIEW)



OUTPUT VOLTAGE
vs
INPUT VOLTAGE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

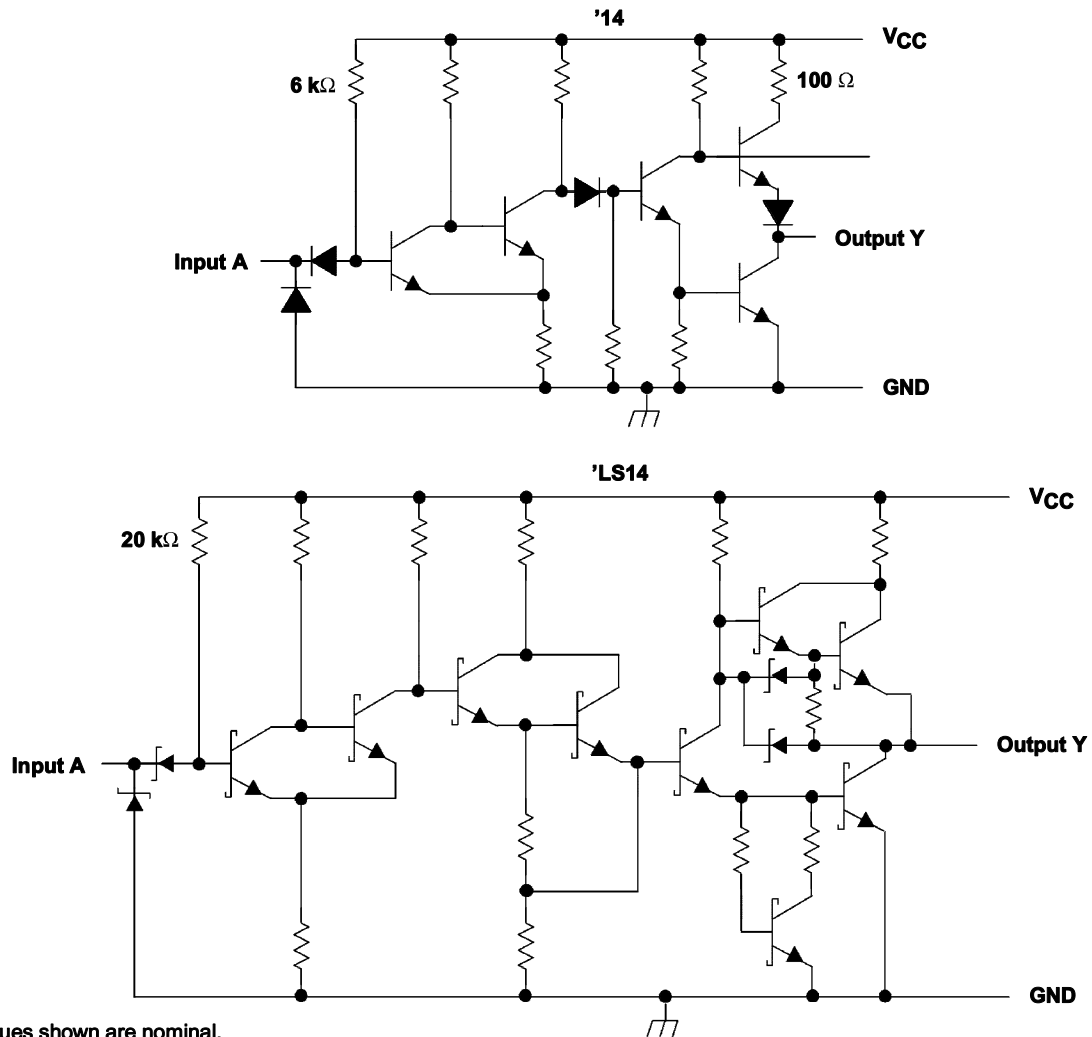
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

schematic



Resistor values shown are nominal.

SN5432, SN54LS32, SN54S32, SN7432, SN74LS32, SN74S32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

DECEMBER 1983 - REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

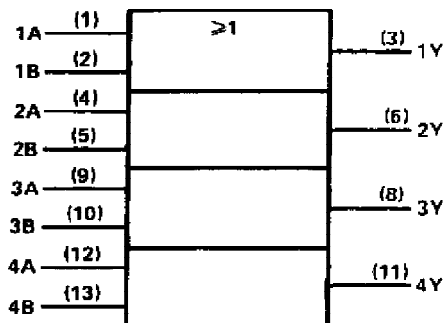
These devices contain four independent 2-input OR gates.

The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of -55°C to 125°C . The SN7432, SN74LS32 and SN74S32 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

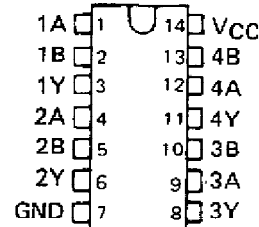
Pin numbers shown are for D, J, N, or W packages.

SN5432, SN54LS32, SN54S32 . . . J OR W PACKAGE

SN7432 . . . N PACKAGE

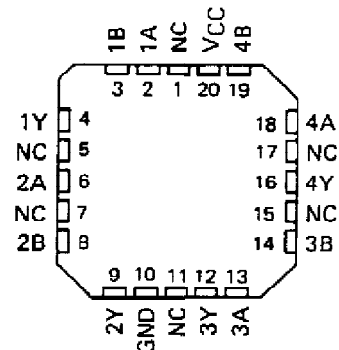
SN74LS32, SN74S32 . . . D OR N PACKAGE

(TOP VIEW)



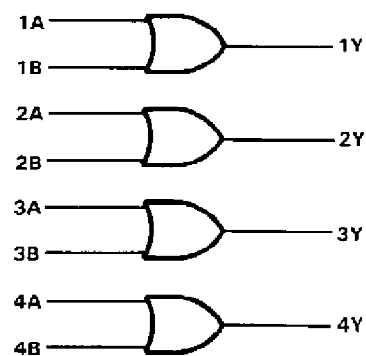
SN54LS32, SN54S32 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

logic diagram



positive logic

$$Y = A + B \text{ or } Y = \overline{\overline{A} \cdot \overline{B}}$$

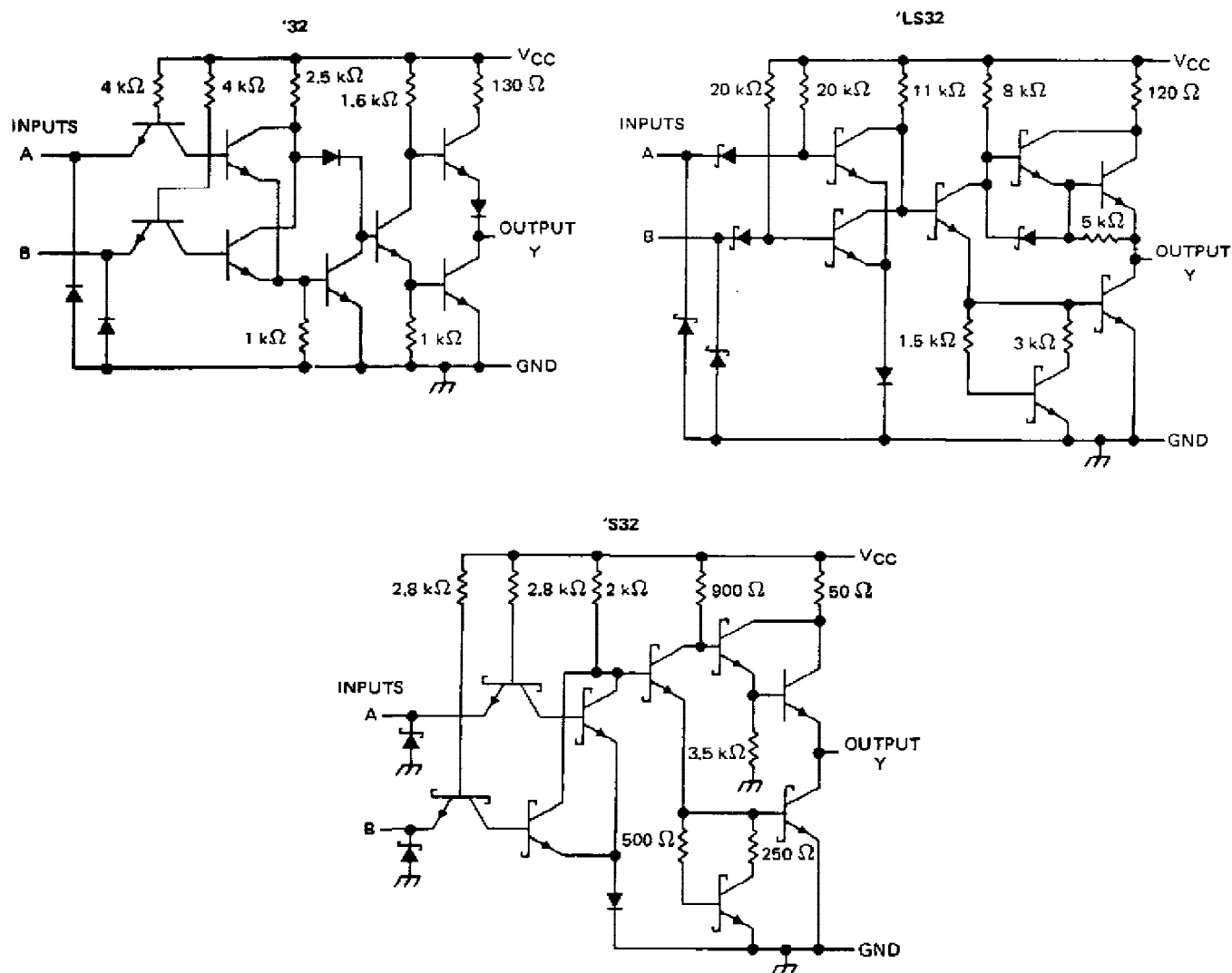
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TEXAS
INSTRUMENTS

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**SN5432, SN54LS32, SN54S32,
SN7432, SN74LS32, SN74S32
QUADRUPLE 2-INPUT POSITIVE-OR GATES**

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---------------------------------------|--|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: '32, 'S32 | 5.5 V |
| 'LS32 | 7 V |
| Operating free-air temperature: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN5445, SN7445 BCD-TO-DECIMAL DECODERS/DRIVERS

SDLS110

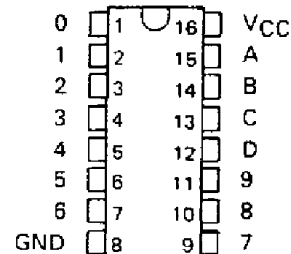
DECEMBER 1972—REVISED MARCH 1988

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

featuring

- Full Decoding of Input Logic
- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

SN5445 . . . J OR W PACKAGE
SN7445 . . . N PACKAGE
(TOP VIEW)



FUNCTION TABLE

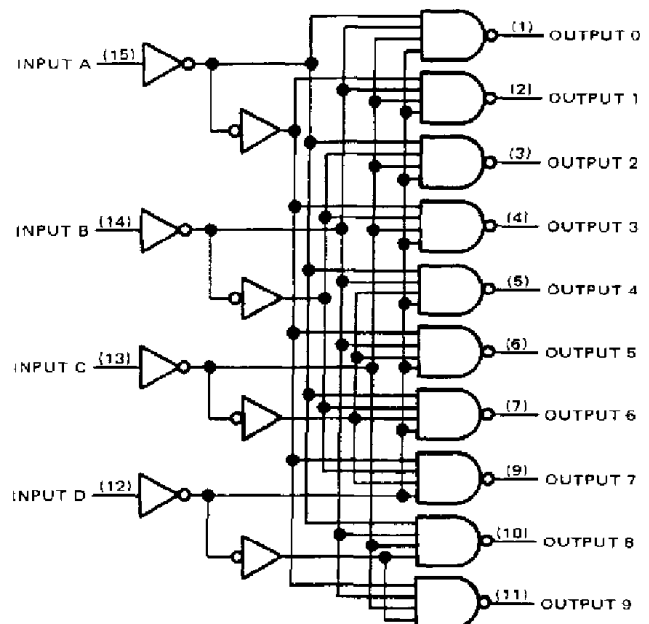
| NO. | INPUTS | | | | OUTPUTS | | | | | | | | | |
|---------|--------|---|---|---|---------|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| 1 | L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| 2 | L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| 3 | L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| 4 | L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| 5 | L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| 6 | L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| 7 | L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| 9 | H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| INVALID | H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | L | H | H | H | H | H | H | H | H | H | H |

H = high level (off), L = low level (on)

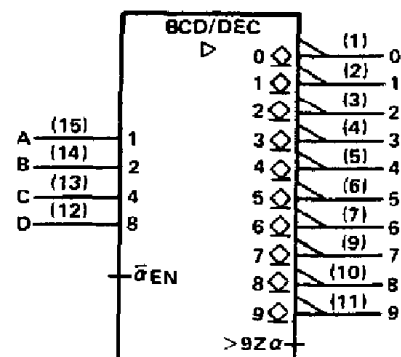
description

These monolithic BCD-to-decimal decoders/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (30 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

logic diagram (positive logic)



logic symbol



OPEN-COLLECTOR OUTPUTS

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TEXAS
INSTRUMENTS

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SN5474, SN54LS74A, SN54S74 SN7474, SN74LS74A, SN74S74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

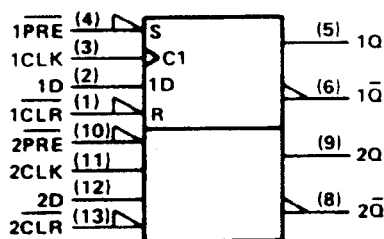
The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|--------|-----|-----|---|----------------|----------------|
| PRE | CLR | CLK | D | Q | \bar{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H [†] | H [†] |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | Q ₀ | \bar{Q}_0 |

[†] The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

logic symbol[‡]

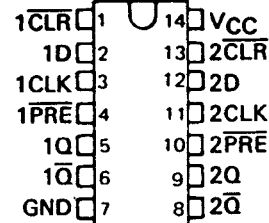


[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

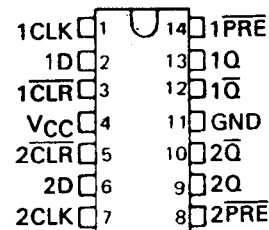
Pin numbers shown are for D, J, N, and W packages.

SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE

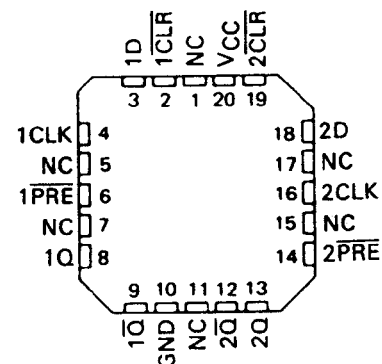
(TOP VIEW)



SN5474 . . . W PACKAGE
(TOP VIEW)

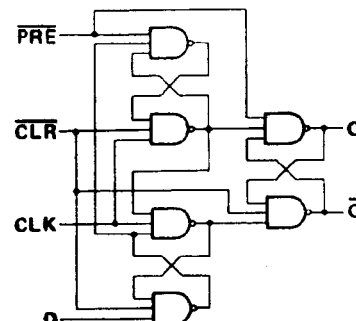


SN54LS74A, SN54S74 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic diagram (positive logic)



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 **TEXAS
INSTRUMENTS**

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SN5476, SN54LS76A SN7476, SN74LS76A DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

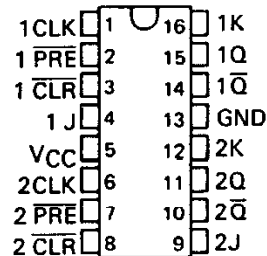
description

The '76 contains two independent J-K flip-flops with individual J-K, clock, preset, and clear inputs. The '76 is a positive-edge-triggered flip-flop. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS76A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predicatble operation. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN5476 and the SN54LS76A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7476 and the SN74LS76A are characterized for operation from 0°C to 70°C .

SN5476, SN54LS76A . . . J PACKAGE
SN7476 . . . N PACKAGE
SN74LS76A . . . D OR N PACKAGE
(TOP VIEW)



'76
FUNCTION TABLE

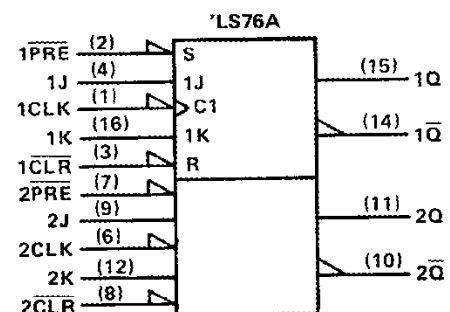
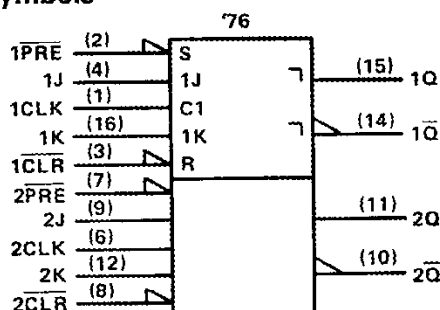
| INPUTS | | | | | OUTPUTS | |
|--------|-----|-----|---|---|----------------|----------------|
| PRE | CLR | CLK | J | K | Q | \bar{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H [†] | H [†] |
| H | H | | L | L | Q ₀ | \bar{Q}_0 |
| H | H | | H | L | H | L |
| H | H | | L | H | L | H |
| H | H | | H | H | TOGGLE | TOGGLE |

'LS76A
FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | |
|--------|-----|-----|---|---|----------------|----------------|
| PRE | CLR | CLK | J | K | Q | \bar{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H [†] | H [†] |
| H | H | | L | L | Q ₀ | \bar{Q}_0 |
| H | H | | H | L | H | L |
| H | H | | L | H | L | H |
| H | H | | H | H | TOGGLE | TOGGLE |
| H | H | H | X | X | Q ₀ | \bar{Q}_0 |

[†] This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high)

logic symbols[†]



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**TEXAS
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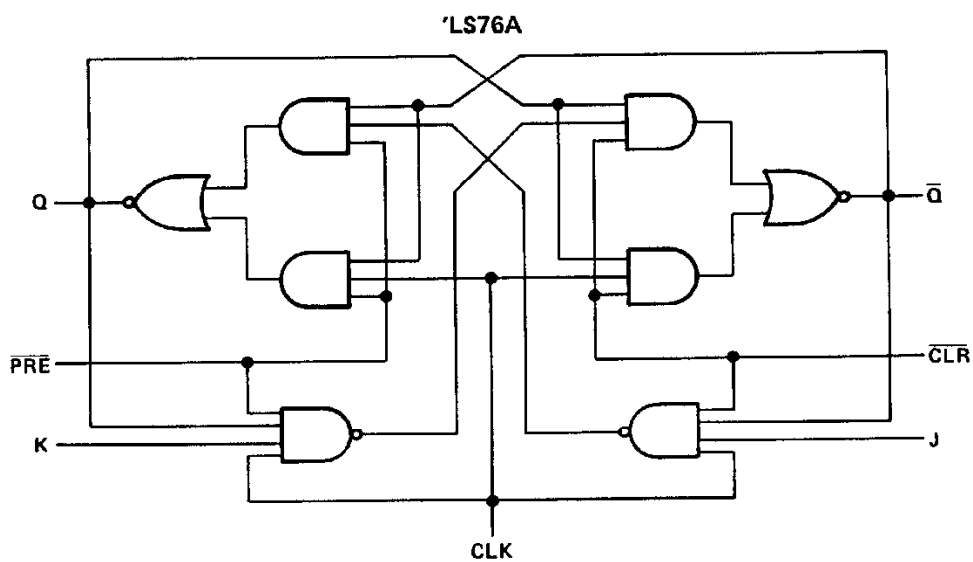
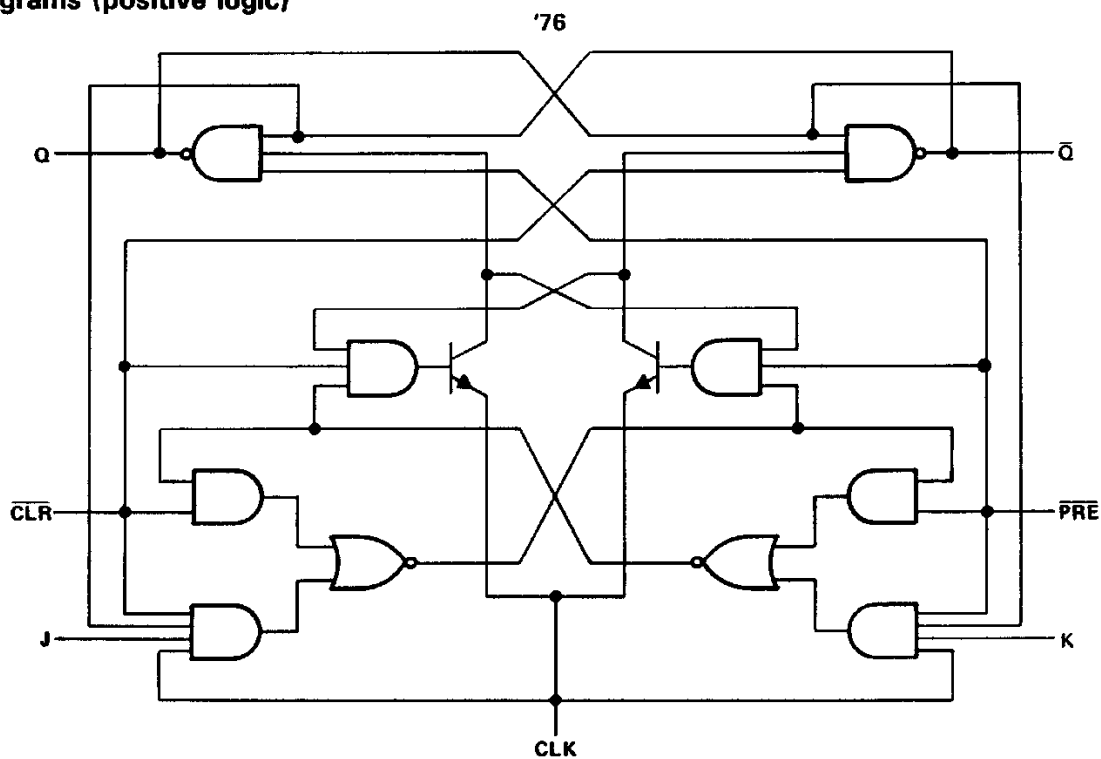
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**SN5476, SN54LS76A
SN7476, SN74LS76A
DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR**

SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

logic diagrams (positive logic)

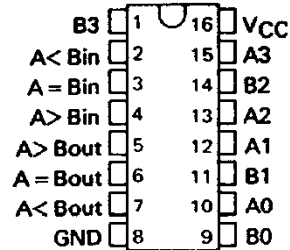


SN5485, SN54LS85, SN54S85 SN7485, SN74LS85, SN74S85 4-BIT MAGNITUDE COMPARATORS

SDLS123 – MARCH 1974 – REVISED MARCH 1988

| TYPE | TYPICAL POWER DISSIPATION | TYPICAL DELAY (4-BIT WORDS) |
|-------|---------------------------------|-----------------------------------|
| '85 | 275 mW | 23 ns |
| 'LS85 | 52 mW | 24 ns |
| 'S85 | 365 mW | 11 ns |

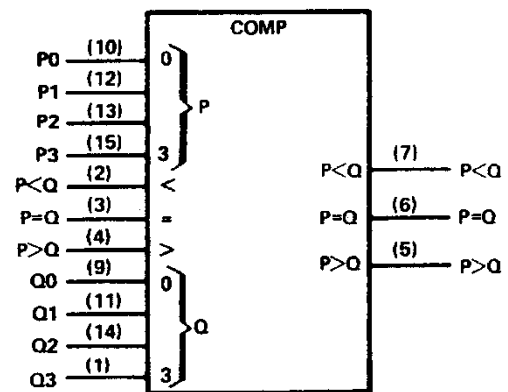
SN5485, SN54LS85, SN54S85 . . . J OR W PACKAGE
SN7485 . . . N PACKAGE
SN74LS85, SN74S85 . . . D OR N PACKAGE
(TOP VIEW)



description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The $A > B$, $A < B$, and $A = B$ outputs of a stage handling less-significant bits are connected to the corresponding $A > B$, $A < B$, and $A = B$ inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the $A = B$ input. The cascading paths of the '85, 'LS85, and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

logic symbol†



†This symbol is in accordance with
ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

| COMPARING INPUTS | | | | CASCADING INPUTS | | | OUTPUTS | | |
|---------------------|---------|---------|---------|---------------------|-------|-------|---------|-------|-------|
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A > B | A < B | A = B | A > B | A < B | A = B |
| A3 > B3 | X | X | X | X | X | X | H | L | L |
| A3 < B3 | X | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 > B2 | X | X | X | X | X | H | L | L |
| A3 = B3 | A2 < B2 | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 > B1 | X | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 < B1 | X | X | X | X | L | H | L |
| A2 = B3 | A2 = B2 | A1 = B1 | A0 > B0 | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 < B0 | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | L | L | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | H | L | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | X | X | H | L | L | H |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | H | L | L | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | L | L | H | H | L |

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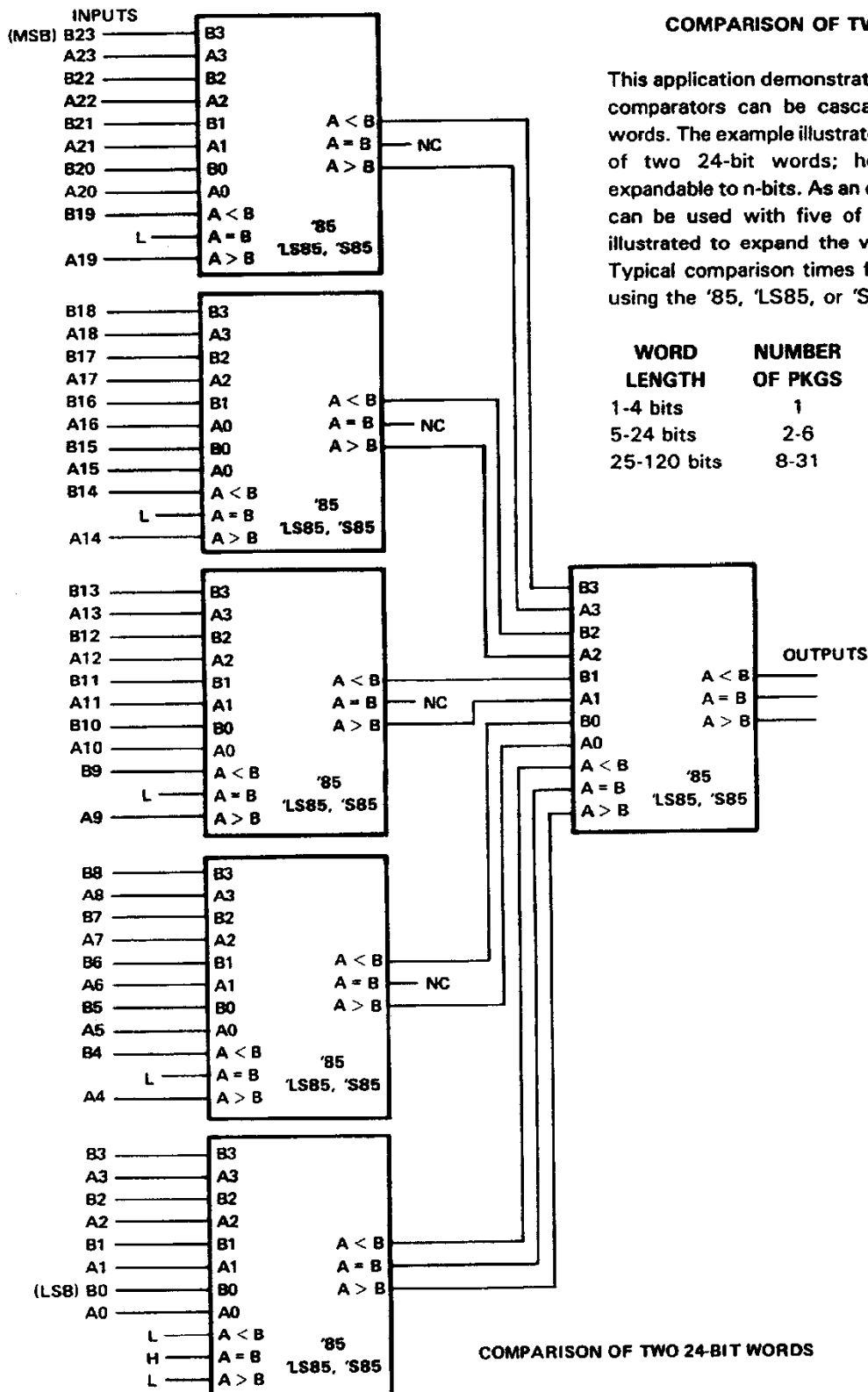
**TEXAS
INSTRUMENTS**

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SN5485, SN54LS85, SN54S85
 SN7485, SN74LS85, SN74S85
4-BIT MAGNITUDE COMPARATORS
 SDLS123 – MARCH 1974 – REVISED MARCH 1988

TYPICAL APPLICATION DATA



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

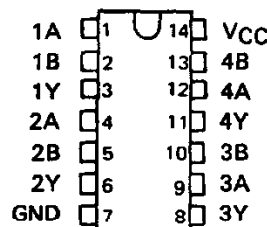
SN5486, SN54LS86A, SN54S86 SN7486, SN74LS86A, SN74S86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SDLS124 – DECEMBER 1972 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN5486, SN54LS86A, SN54S86 . . . J OR W PACKAGE
SN7486 . . . N PACKAGE
SN74LS86A, SN74S86 . . . D OR N PACKAGE

(TOP VIEW)



| TYPE | TYPICAL AVERAGE PROPAGATION DELAY TIME | TYPICAL TOTAL POWER DISSIPATION |
|--------|--|---------------------------------------|
| '86 | 14 ns | 150 mW |
| 'LS86A | 10 ns | 30.5 mW |
| 'S86 | 7 ns | 250 mW |

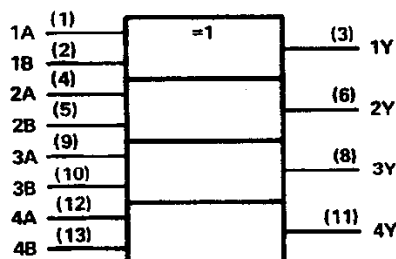
description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN5486, 54LS86A, and the SN54S86 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7486, SN74LS86A, and the SN74S86 are characterized for operation from 0°C to 70°C .

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

H = high level, L = low level

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR



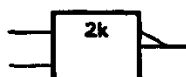
These are five equivalent Exclusive-OR symbols valid for an '86 or 'LS86A gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



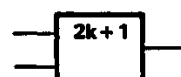
The output is active (low) if all inputs stand at the same logic level (i.e., $A=B$).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

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SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A—MARCH 1974—REVISED MARCH 1988

'90A, 'LS90 . . . Decade Counters

'92A, 'LS92 . . . Divide By-Twelve Counters

'93A, 'LS93 . . . 4-Bit Binary Counters

| TYPES | TYPICAL POWER DISSIPATION |
|---------------------|------------------------------|
| '90A | 145 mW |
| '92A, '93A | 130 mW |
| 'LS90, 'LS92, 'LS93 | 45 mW |

description

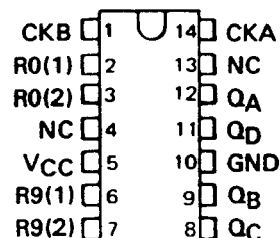
Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and the divide-by-eight for the '93A and 'LS93.

All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the Q_A output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the Q_D output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output Q_A .

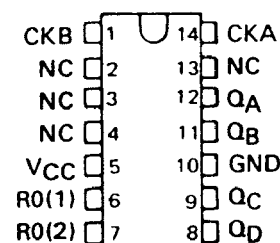
SN5490A, SN54LS90 . . . J OR W PACKAGE
SN7490A . . . N PACKAGE
SN74LS90 . . . D OR N PACKAGE

(TOP VIEW)



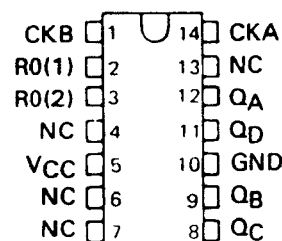
SN5492A, SN54LS92 . . . J OR W PACKAGE
SN7492A . . . N PACKAGE
SN74LS92 . . . D OR N PACKAGE

(TOP VIEW)



SN5493A, SN54LS93 . . . J OR W PACKAGE
SN7493 . . . N PACKAGE
SN74LS93 . . . D OR N PACKAGE

(TOP VIEW)



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 **TEXAS
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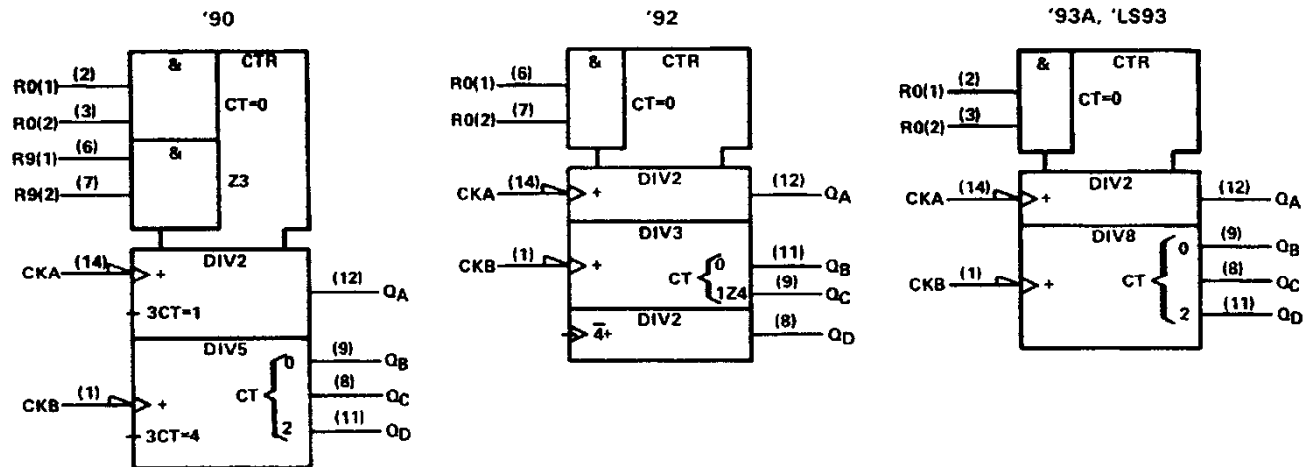
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SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

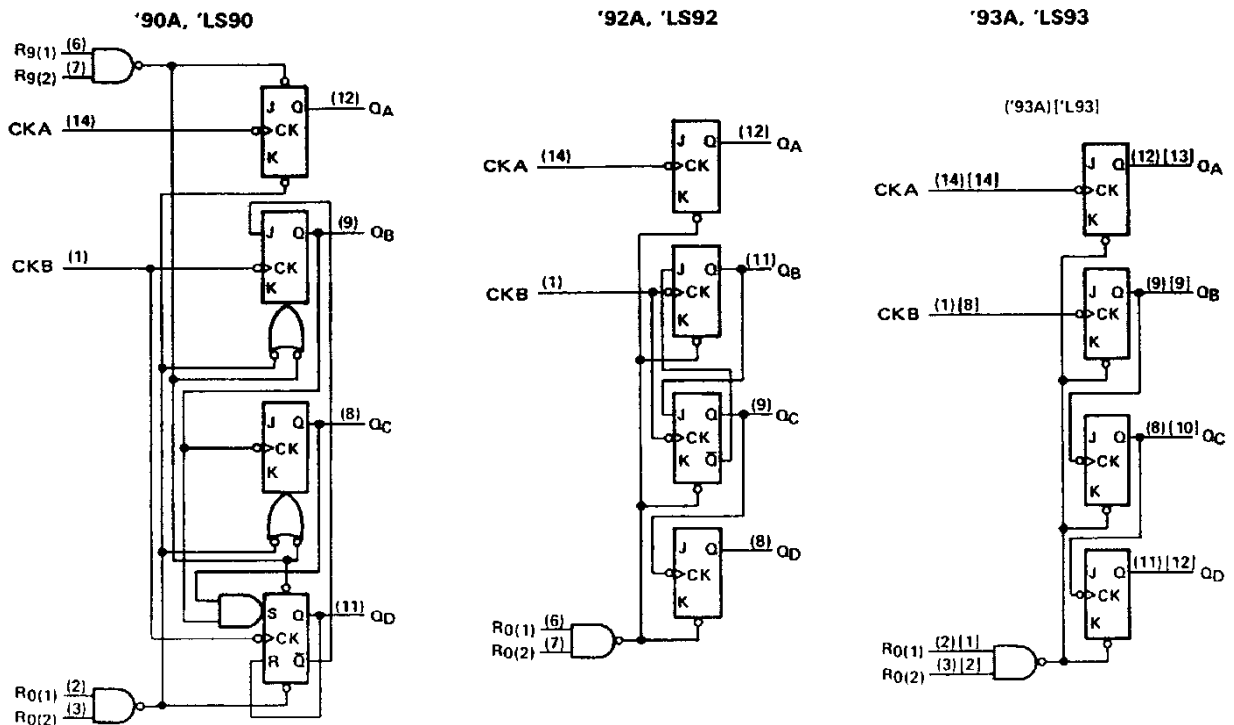
SDL940A – MARCH 1974 – REVISED MARCH 1988

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



The J and K inputs shown without connection are for reference only and are functionally at a high level.
Pin numbers shown in () are for the 'LS93 and '93A and pin numbers shown in [] are for the 54L93.



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**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A—MARCH 1974—REVISED MARCH 1988

**'90A, 'LS90
BCD COUNT SEQUENCE
(See Note A)**

| COUNT | OUTPUT | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _D | Q _C | Q _B | Q _A |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

**'90A, 'LS90
BI-QUINARY (5-2)
(See Note B)**

| COUNT | OUTPUT | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _A | Q _D | Q _C | Q _B |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

**'92A, 'LS92
COUNT SEQUENCE
(See Note C)**

| COUNT | OUTPUT | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _D | Q _C | Q _B | Q _A |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | H | L | L | L |
| 7 | H | L | L | H |
| 8 | H | L | H | L |
| 9 | H | L | H | H |
| 10 | H | H | L | L |
| 11 | H | H | L | H |

**'90A, 'LS90
RESET/COUNT FUNCTION TABLE**

| RESET INPUTS | | | | OUTPUT | | | |
|--------------------|--------------------|--------------------|--------------------|----------------|----------------|----------------|----------------|
| R ₀ (1) | R ₀ (2) | R ₉ (1) | R ₉ (2) | Q _D | Q _C | Q _B | Q _A |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| X | L | X | L | COUNT | | | |
| L | X | L | X | COUNT | | | |
| L | X | X | L | COUNT | | | |
| X | L | L | X | COUNT | | | |

**'93A, 'LS93
COUNT SEQUENCE
(See Note C)**

| COUNT | OUTPUT | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _D | Q _C | Q _B | Q _A |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

**'92A, 'LS92, '93A, 'LS93
RESET/COUNT FUNCTION TABLE**

| RESET INPUTS | | OUTPUT | | | |
|--------------------|--------------------|----------------|----------------|----------------|----------------|
| R ₀ (1) | R ₀ (2) | Q _D | Q _C | Q _B | Q _A |
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |

- NOTES: A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKA for bi-quinary count.
C. Output Q_A is connected to input CKB.
D. H = high level, L = low level, X = irrelevant



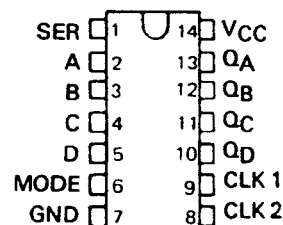
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SN5495A, SN54LS95B SN7495A, SN74LS95B 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

SDLS128 - MARCH 1974 - REVISED MARCH 1988

| TYPE | TYPICAL MAXIMUM CLOCK FREQUENCY | TYPICAL POWER DISSIPATION |
|--------|------------------------------------|------------------------------|
| '95A | 36 MHz | 195 mW |
| 'LS95B | 36 MHz | 65 mW |

SN5495A, SN54LS95B . . . J OR W PACKAGE
SN7495A . . . N PACKAGE
SN74LS95B . . . D OR N PACKAGE
(TOP VIEW)



description

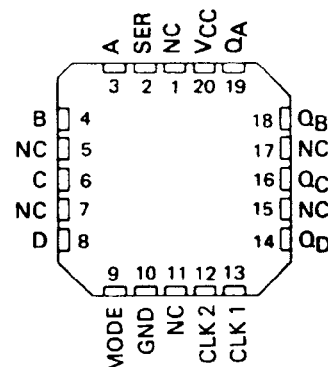
These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

- Parallel (broadside) load
- Shift right (the direction Q_A toward Q_D)
- Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

SN54LS95B . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

| MODE CONTROL | CLOCKS | | INPUTS | | | | | OUTPUTS | | | |
|-----------------|--------|-------|--------|----------|----------|----------|---|----------|----------|----------|----------|
| | 2 (L) | 1 (R) | SERIAL | PARALLEL | | | | Q_A | Q_B | Q_C | Q_D |
| | | | | A | B | C | D | | | | |
| H | H | X | X | X | X | X | X | Q_{A0} | Q_{B0} | Q_{C0} | Q_{D0} |
| H | ↓ | X | X | a | b | c | d | a | b | c | d |
| H | ↓ | X | X | $Q_{B†}$ | $Q_{C†}$ | $Q_{D†}$ | d | Q_{Bn} | Q_{Cn} | Q_{Dn} | d |
| L | L | H | X | X | X | X | X | Q_{A0} | Q_{B0} | Q_{C0} | Q_{D0} |
| L | X | ↓ | H | X | X | X | X | H | Q_{An} | Q_{Bn} | Q_{Cn} |
| L | X | ↓ | L | X | X | X | X | L | Q_{An} | Q_{Bn} | Q_{Cn} |
| ↑ | L | L | X | X | X | X | X | Q_{A0} | Q_{B0} | Q_{C0} | Q_{D0} |
| ↓ | L | L | X | X | X | X | X | Q_{A0} | Q_{B0} | Q_{C0} | Q_{D0} |
| ↓ | L | H | X | X | X | X | X | Q_{A0} | Q_{B0} | Q_{C0} | Q_{D0} |
| ↑ | H | L | X | X | X | X | X | Q_{A0} | Q_{B0} | Q_{C0} | Q_{D0} |
| ↑ | H | H | X | X | X | X | X | Q_{A0} | Q_{B0} | Q_{C0} | Q_{D0} |

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established.

Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the most-recent ↓ transition of the clock.

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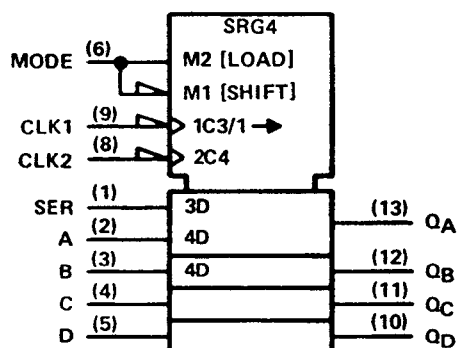
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SN5495A, SN54LS95B SN7495A, SN74LS95B 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

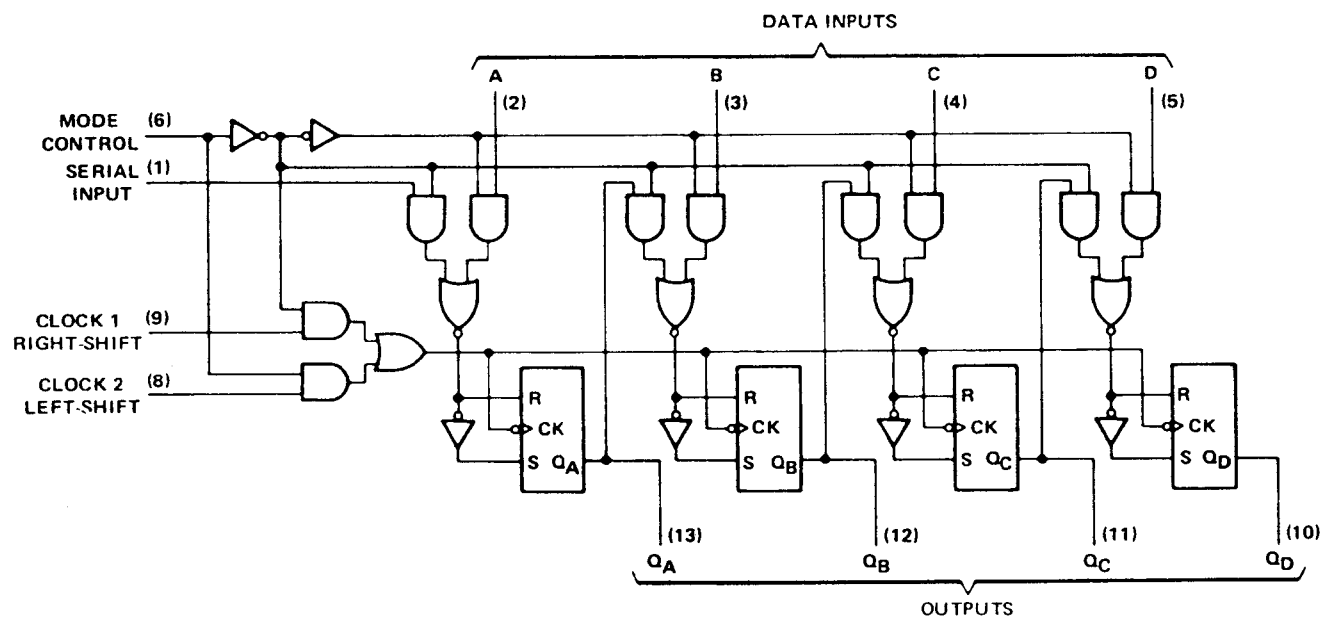
SDLS128—MARCH 1974—REVISED MARCH 1988

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

SN54125, SN54126, SN54LS125A, SN54LS126A, SN74125, SN74126, SN74LS125A, SN74LS126A QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SDLS044A – DECEMBER 1983 – REVISED MARCH 2002

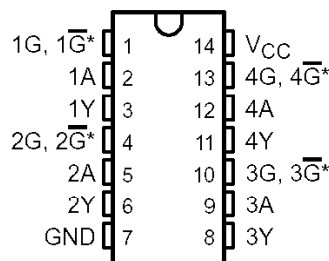
- Quad Bus Buffers
- 3-State Outputs
- Separate Control for Each Channel

description

These bus buffers feature three-state outputs that, when enabled, have the low impedance characteristics of a TTL output with additional drive capability at high logic levels to permit driving heavily loaded bus lines without external pullup resistors. When disabled, both output transistors are turned off, presenting a high-impedance state to the bus so the output will act neither as a significant load nor as a driver. The '125 and 'LS125A devices' outputs are disabled when \overline{G} is high. The '126 and 'LS126A devices' outputs are disabled when G is low.

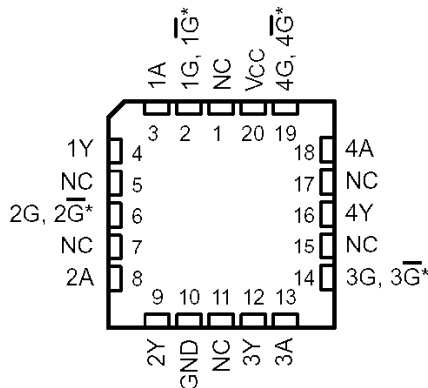
SN54125, SN54126, SN54LS125A,
SN54LS126A . . . J OR W PACKAGE
SN74125, SN74126 . . . N PACKAGE
SN74LS125A, SN74LS126A . . . D, N, OR NS PACKAGE

(TOP VIEW)



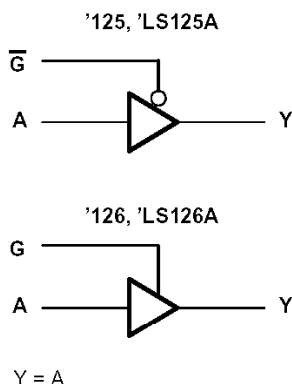
* \overline{G} on '125 and 'LS125A devices;
G on '126 and 'LS126A devices

SN54LS125A, SN54LS126A . . . FK PACKAGE
(TOP VIEW)

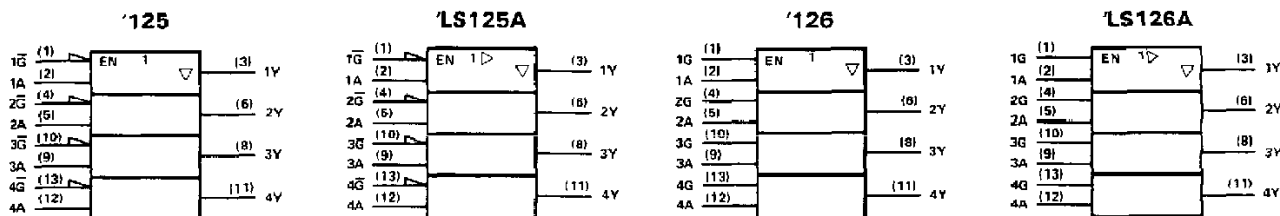


* \overline{G} on '125 and 'LS125A devices;
G on '126 and 'LS126A devices
- No internal connection

logic diagram (each gate)



logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

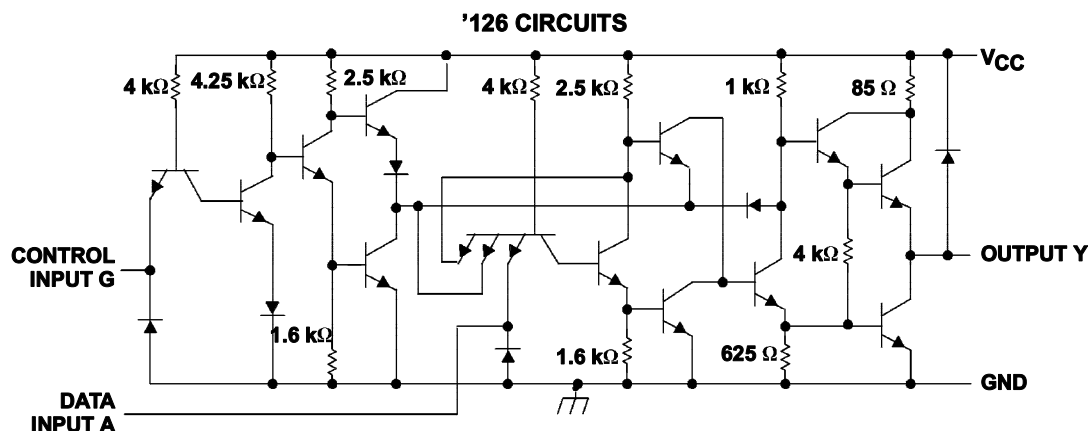
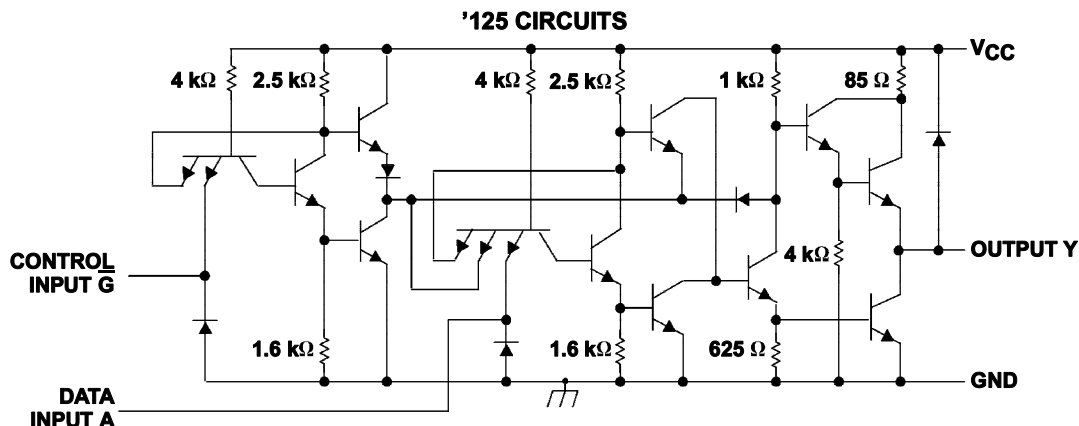
The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

SN54125, SN54126, SN54LS125A, SN54LS126A, SN74125, SN74126, SN74LS125A, SN74LS126A

QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SDLS044A – DECEMBER 1983 – REVISED MARCH 2002

schematics (each gate)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]
(^{'125} and ^{'126})

| | |
|--|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage, V_I | 5.5 V |
| Package thermal impedance, θ_{JA} (see Note 2): N package | 80°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LS138, SN54S138, SN74LS138, SN74S138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

SDLS014

DECEMBER 1972—REVISED MARCH 1988

- Designed Specifically for High-Speed: Memory Decoders Data Transmission Systems
- 3 Enable Inputs to Simplify Cascading and/or Data Reception
- Schottky-Clamped for High Performance

description

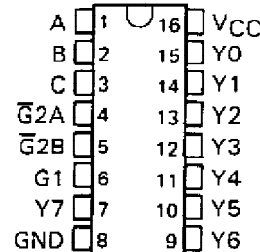
These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138, SN54S138, and SN74S138A decode one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

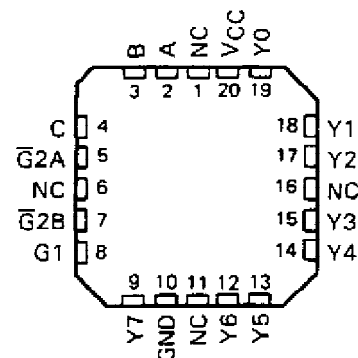
All of these decoder/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design.

The SN54LS138 and SN54S138 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS138 and SN74S138A are characterized for operation from 0°C to 70°C .

SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138A . . . D OR N PACKAGE
(TOP VIEW)

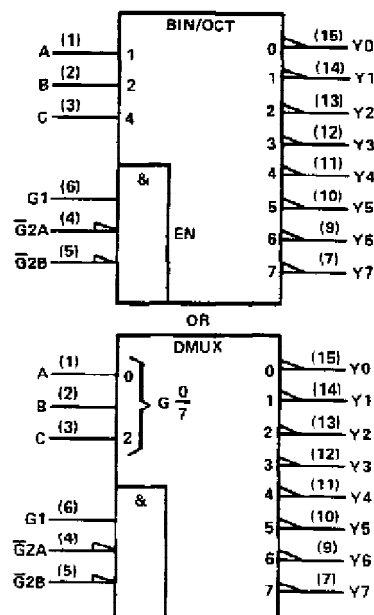


SN54LS138, SN54S138 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

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TEXAS
INSTRUMENTS

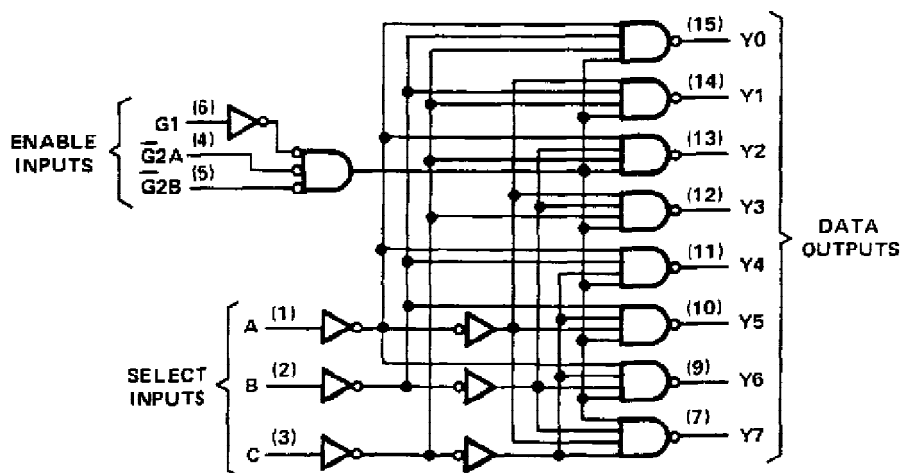
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SN54LS138, SN54S138, SN74LS138, SN74S138A **3-LINE-TO 8-LINE DECODERS/DEMULTIPLEXERS**

logic diagram and function table

'LS138, SN54S138, SN74S138A



Pin numbers shown are for D, J, N, and W packages.

'LS138, SN54138, SN74S138A

FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | | | | | | | |
|--------|-----|--------|---|---|---------|----|----|----|----|----|----|----|
| ENABLE | | SELECT | | | | | | | | | | |
| G1 | G2* | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | L | H | H | H | H | H |
| H | L | L | L | L | H | H | H | L | H | H | H | H |
| H | L | L | L | H | H | H | H | L | H | H | H | H |
| H | L | L | L | L | H | H | H | H | L | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H |
| H | L | L | L | L | H | H | H | H | H | L | H | H |
| H | L | L | L | H | H | H | H | H | H | H | L | H |
| H | L | L | L | L | H | H | H | H | H | H | H | L |

$$*G2 = G2A + G2B$$

H = high level, L = low level, X = irrelevant

TEXAS
INSTRUMENTS

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SN54LS139A, SN54S139, SN74LS139A, SN74S139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

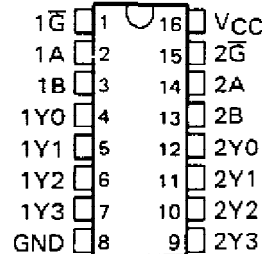
SDLS013

DECEMBER 1972 - REVISED MARCH 1988

- Designed Specifically for High-Speed:
Memory Decoders
Data Transmission Systems
- Two Fully Independent 2- to 4-Line
Decoders/Demultiplexers
- Schottky Clamped for High Performance

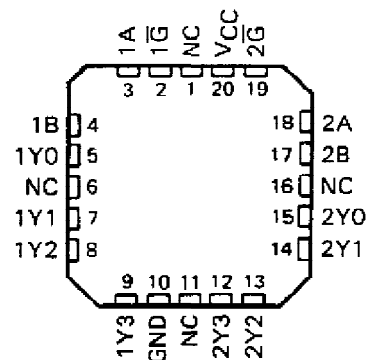
SN54LS139A, SN54S139 ... J OR W PACKAGE
SN74LS139A, SN74S139A ... D OR N PACKAGE

(TOP VIEW)



SN54LS139A, SN54S139 ... FK PACKAGE

(TOP VIEW)



NC—No internal connection

description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The circuit comprises two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

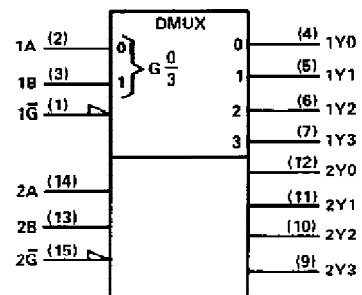
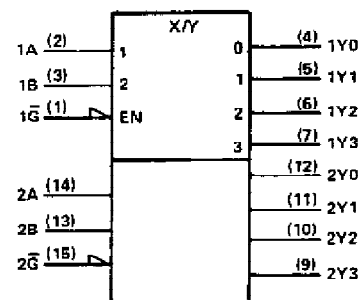
All of these decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design. The SN54LS139A and SN54S139 are characterized for operation range of -55°C to 125°C . The SN74LS139A and SN74S139A are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

| INPUTS | | OUTPUTS | | | |
|-----------------------|--------|---------|----|----|----|
| ENABLE | SELECT | | | | |
| $\overline{\text{G}}$ | B A | Y0 | Y1 | Y2 | Y3 |
| H | X X | H | H | H | H |
| L | L L | L | H | H | H |
| L | L H | H | L | H | H |
| L | H L | H | H | L | H |
| L | H H | H | H | H | L |

H = high level, L = low level, X = irrelevant

logic symbols (alternatives)[†]



[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

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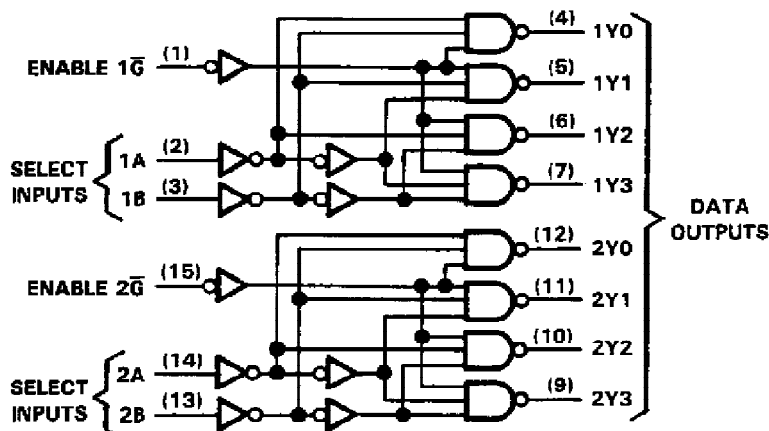
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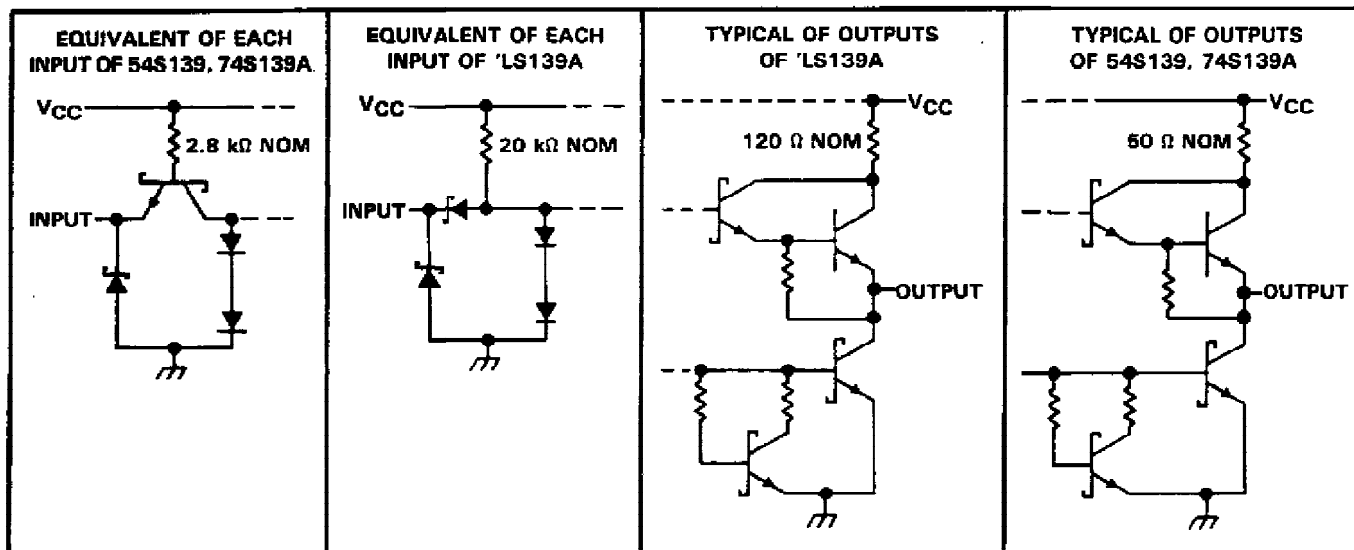
SN54LS139A, SN54S139, SN74LS139A, SN74S139A **DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS**

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--|----------------|
| Supply voltage, V_{CC} (See Note 1) | 7 V |
| Input voltage: 'LS139A | 7 V |
| 54S139, 74S139A | 5.5 V |
| Operating free-air temperature range: SN54LS139A, SN54S139 | -55°C to 125°C |
| SN74LS139A, SN74S139A | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SN54150, SN54151A, SN54LS151, SN54S151, SN74150, SN74151A, SN74LS151, SN74S151 DATA SELECTORS/MULTIPLEXERS

DECEMBER 1972—REVISED MARCH 1988

- '150 Selects One-of-Sixteen Data Sources
- Others Select One-of-Eight Data Sources
- All Perform Parallel-to-Serial Conversion
- All Permit Multiplexing from N Lines to One Line
- Also For Use as Boolean Function Generator
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL Circuits

| TYPE | TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT | TYPICAL POWER DISSIPATION |
|--------|---|---------------------------------|
| '150 | 13 ns | 200 mW |
| '151A | 8 ns | 145 mW |
| 'LS151 | 13 ns | 30 mW |
| 'S151 | 4.5 ns | 225 mW |

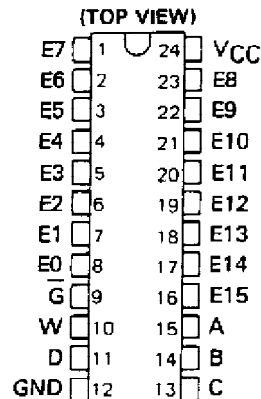
description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired data source. The '150 selects one-of-sixteen data sources; the '151A, 'LS151, and 'S151 select one-of-eight data sources. The '150, '151A, 'LS151, and 'S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

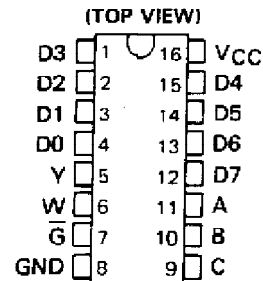
The '150 has only an inverted W output; the '151A, 'LS151, and 'S151 feature complementary W and Y outputs.

The '151A and '152A incorporate address buffers that have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the '151A outputs are enabled (i.e., strobe low).

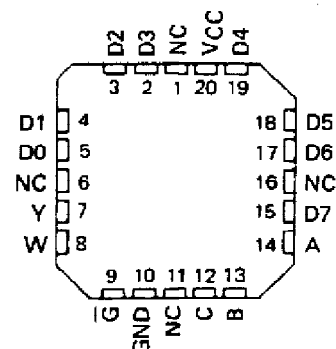
SN54150 . . . J OR W PACKAGE
SN74150 . . . N PACKAGE



SN54151A, SN54LS151, SN54S151 . . . J OR W PACKAGE
SN74151A . . . N PACKAGE
SN74LS151, SN74S151 . . . D OR N PACKAGE



SN54LS151, SN54S151 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

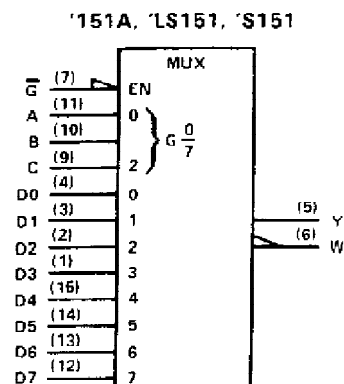
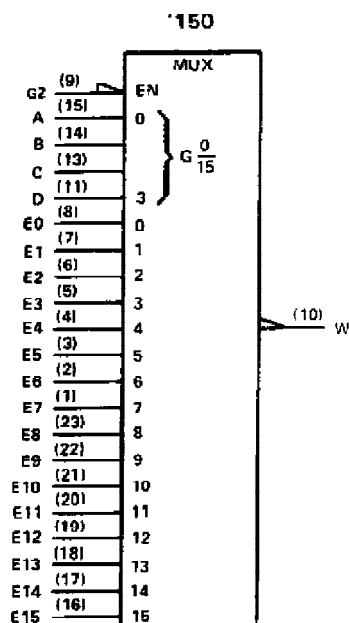
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SN54150, SN54151A, SN54LS151, SN54S151, SN74150, SN74151A, SN74LS151, SN74S151 DATA SELECTORS/MULTIPLEXERS

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are D, J, N, and W packages.

'150

FUNCTION TABLE

| INPUTS | | | | STROBE \bar{G} | OUTPUT W |
|-------------|---|---|---|---------------------|-------------|
| SELECT D | C | B | A | | |
| X | X | X | X | H | H |
| L | L | L | L | L | $\bar{E0}$ |
| L | L | L | H | L | $\bar{E1}$ |
| L | L | H | L | L | $\bar{E2}$ |
| L | L | H | H | L | $\bar{E3}$ |
| L | H | L | L | L | $\bar{E4}$ |
| L | H | L | H | L | $\bar{E5}$ |
| L | H | H | L | L | $\bar{E6}$ |
| L | H | H | H | L | $\bar{E7}$ |
| H | L | L | L | L | $\bar{E8}$ |
| H | L | L | H | L | $\bar{E9}$ |
| H | L | H | L | L | $\bar{E10}$ |
| H | L | H | H | L | $\bar{E11}$ |
| H | H | L | L | L | $\bar{E12}$ |
| H | H | L | H | L | $\bar{E13}$ |
| H | H | H | L | L | $\bar{E14}$ |
| H | H | H | H | L | $\bar{E15}$ |

'151A, 'LS151, 'S151

FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|--------|---|---|---------------------|---------|------------|
| SELECT | | | STROBE \bar{G} | Y | W |
| C | B | A | | | |
| X | X | X | H | L | H |
| L | L | L | L | D0 | $\bar{D0}$ |
| L | L | H | L | D1 | $\bar{D1}$ |
| L | H | L | L | D2 | $\bar{D2}$ |
| L | H | H | L | D3 | $\bar{D3}$ |
| H | L | L | L | D4 | $\bar{D4}$ |
| H | L | H | L | D5 | $\bar{D5}$ |
| H | H | L | L | D6 | $\bar{D6}$ |
| H | H | H | L | D7 | $\bar{D7}$ |

H = high level, L = low level, X = irrelevant
 $\bar{E0}, \bar{E1} \dots \bar{E15}$ = the complement of the level of the respective E input
D0, D1 . . . D7 = the level of the D respective input

**TEXAS
INSTRUMENTS**

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SN54LS183, SN74LS183 DUAL CARRY-SAVE FULL ADDERS

SDLS137

BULLETIN NO. DL-57711848, OCTOBER 1976—REVISED MARCH 1988

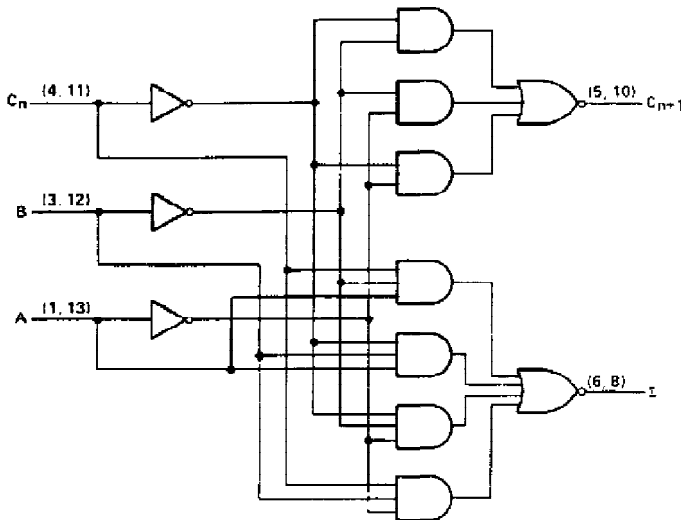
- For Use in High-Speed Wallace-Tree Summing Networks
- High-Speed, High-Fan-Out Darlington Outputs
- Input Clamping Diodes Simplify System Design

| TYPES | TYPICAL AVERAGE PROPAGATION DELAY TIME | TYPICAL POWER DISSIPATION |
|--------|--|---------------------------------|
| 'LS183 | 15 ns | 23 mW per bit |

description

These dual full adders feature an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than two gate delays. The circuits utilize high-speed, high-fan-out, transistor-transistor logic (TTL), but are compatible with both DTL and TTL families. SN54LS183 is characterized for operation over the full military temperature range of -55°C to 125°C ; SN74LS183 is characterized for operation from 0°C to 70°C .

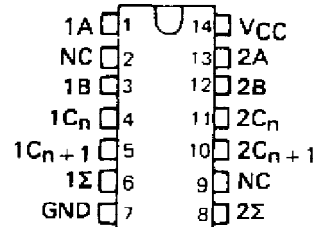
logic diagram (each adder)



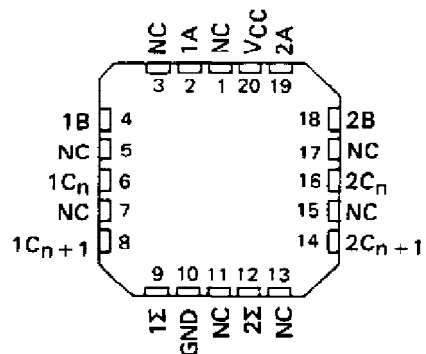
Pin numbers shown are for D, J, N, and W packages.

SN54LS183 . . . J OR W PACKAGE
SN74LS183 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS183 . . . FK PACKAGE
(TOP VIEW)



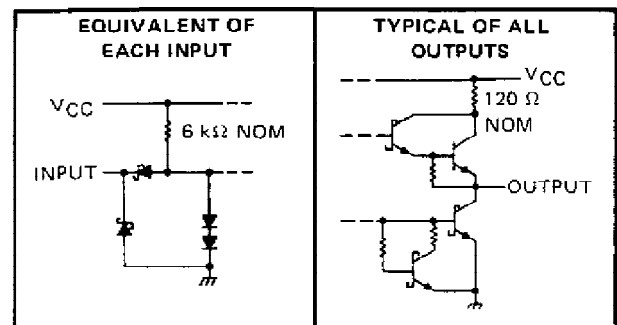
NC - No internal connection

FUNCTION TABLE
(EACH ADDER)

| INPUTS | | | OUTPUTS | |
|--------|---|---|----------|-----------|
| C_n | B | A | Σ | C_{n+1} |
| L | L | L | L | L |
| L | L | H | H | L |
| L | H | L | H | L |
| L | H | H | L | H |
| H | L | L | H | L |
| H | L | H | L | H |
| H | H | L | L | H |
| H | H | H | H | H |

H = high level, L = low level

schematics of inputs and outputs



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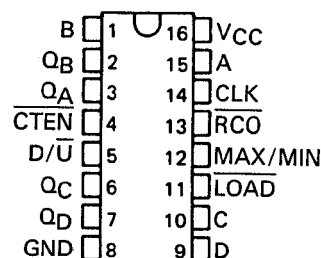
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SN54190, SN54191, SN54LS190, SN54LS191, SN74190, SN74191, SN74LS190, SN74LS191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SDLS072 – DECEMBER 1972 – REVISED MARCH 1988

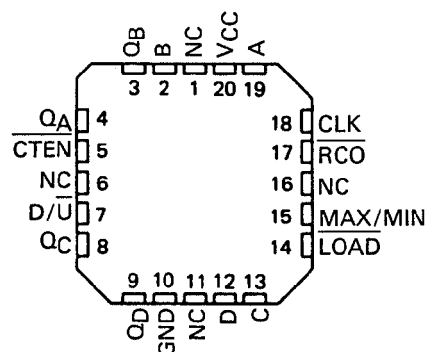
- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presetable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications

SN54190, SN54191, SN54LS190,
SN54LS191 . . . J PACKAGE
SN74190, SN74191 . . . N PACKAGE
SN74LS190, SN74LS191 . . . D OR N PACKAGE
(TOP VIEW)



| TYPE | AVERAGE PROPAGATION DELAY | TYPICAL MAXIMUM CLOCK FREQUENCY | TYPICAL POWER DISSIPATION |
|----------------|---------------------------------|--|---------------------------------|
| '190, '191 | 20ns | 25MHz | 325mW |
| 'LS190, 'LS191 | 20ns | 25MHz | 100mW |

SN54LS190, SN54LS191 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

description

The '190, 'LS190, '191, and 'LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and 'LS191 are 4-bit binary counters and the '190 and 'LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter count up and when high, it counts down. A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Series 54' and 54LS' are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74' and 74LS' are characterized for operation from 0°C to 70°C .

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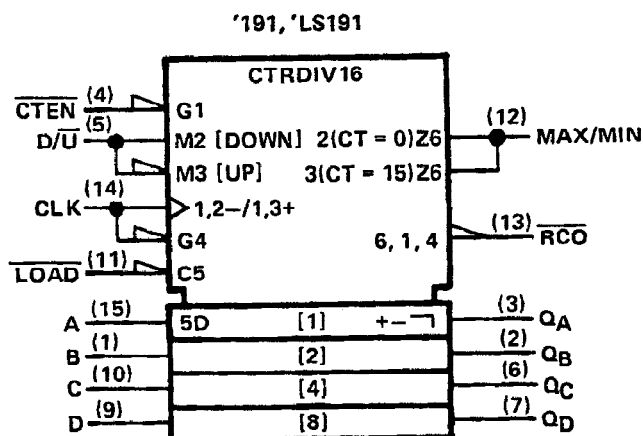
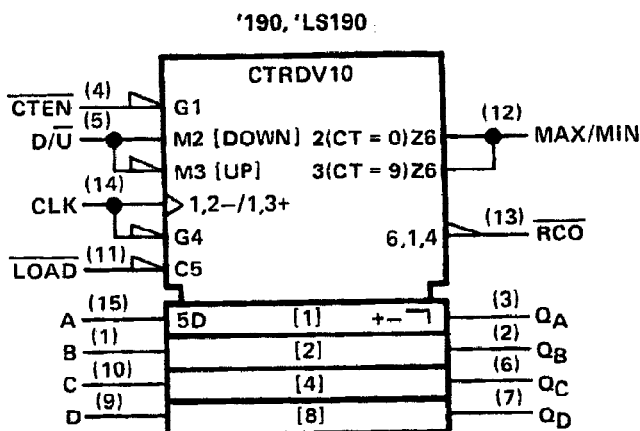
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**SN54190, SN54191, SN54LS190, SN54LS191,
SN74190, SN74191, SN74LS190, SN74LS191**
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL
SDLS072 – DECEMBER 1972 – REVISED MARCH 1988

logic symbols†



† These symbols are accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

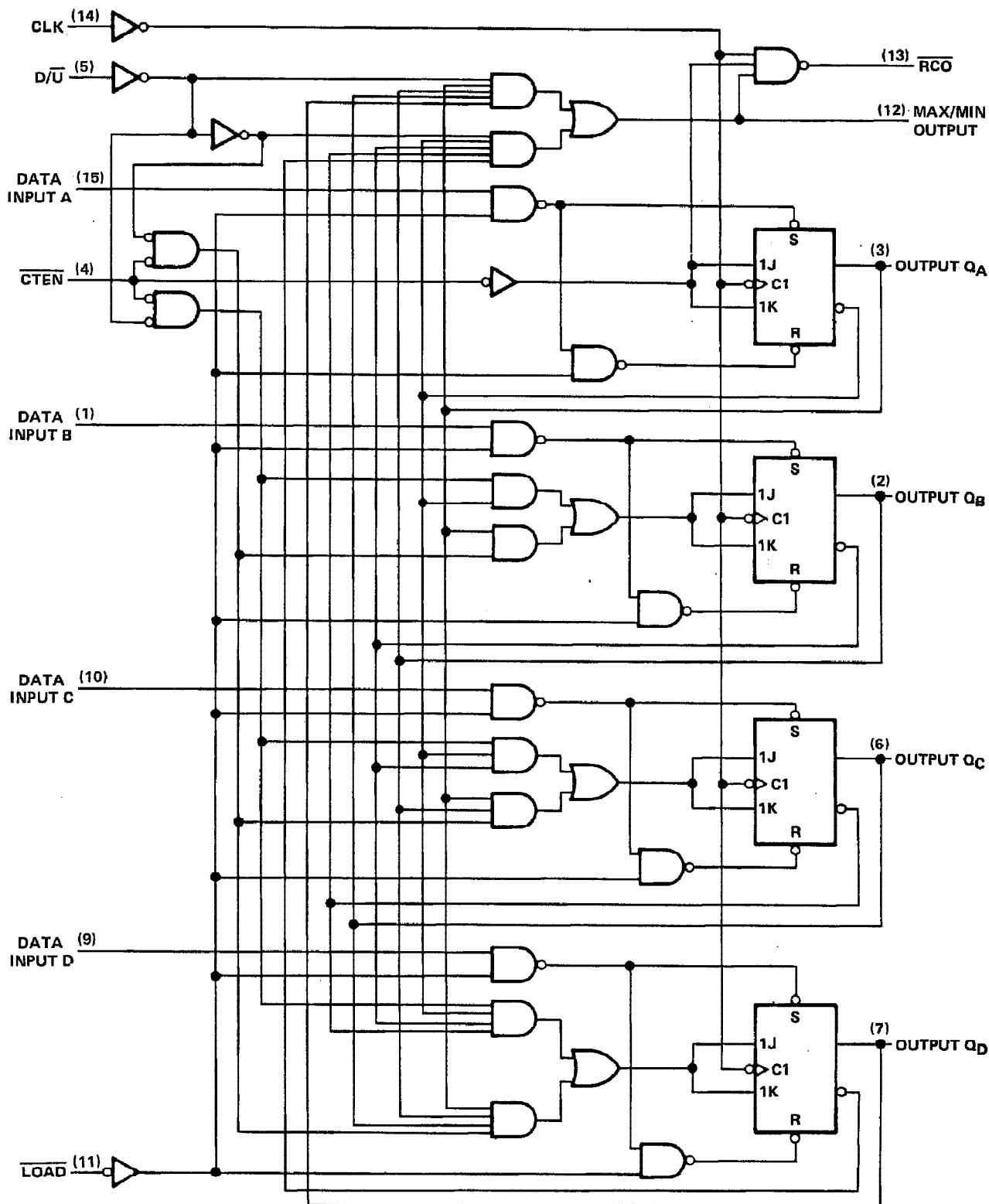
SN54191, SN54LS191, SN74191, SN74LS191

SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SDLS072 – DECEMBER 1972 – REVISED MARCH 1988

logic diagram (positive logic)

'191, 'LS191 BINARY COUNTERS



Pin numbers shown are for D, J, and N packages.

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INSTRUMENTS**

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SN54191, SN54LS191, SN74191, SN74LS191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

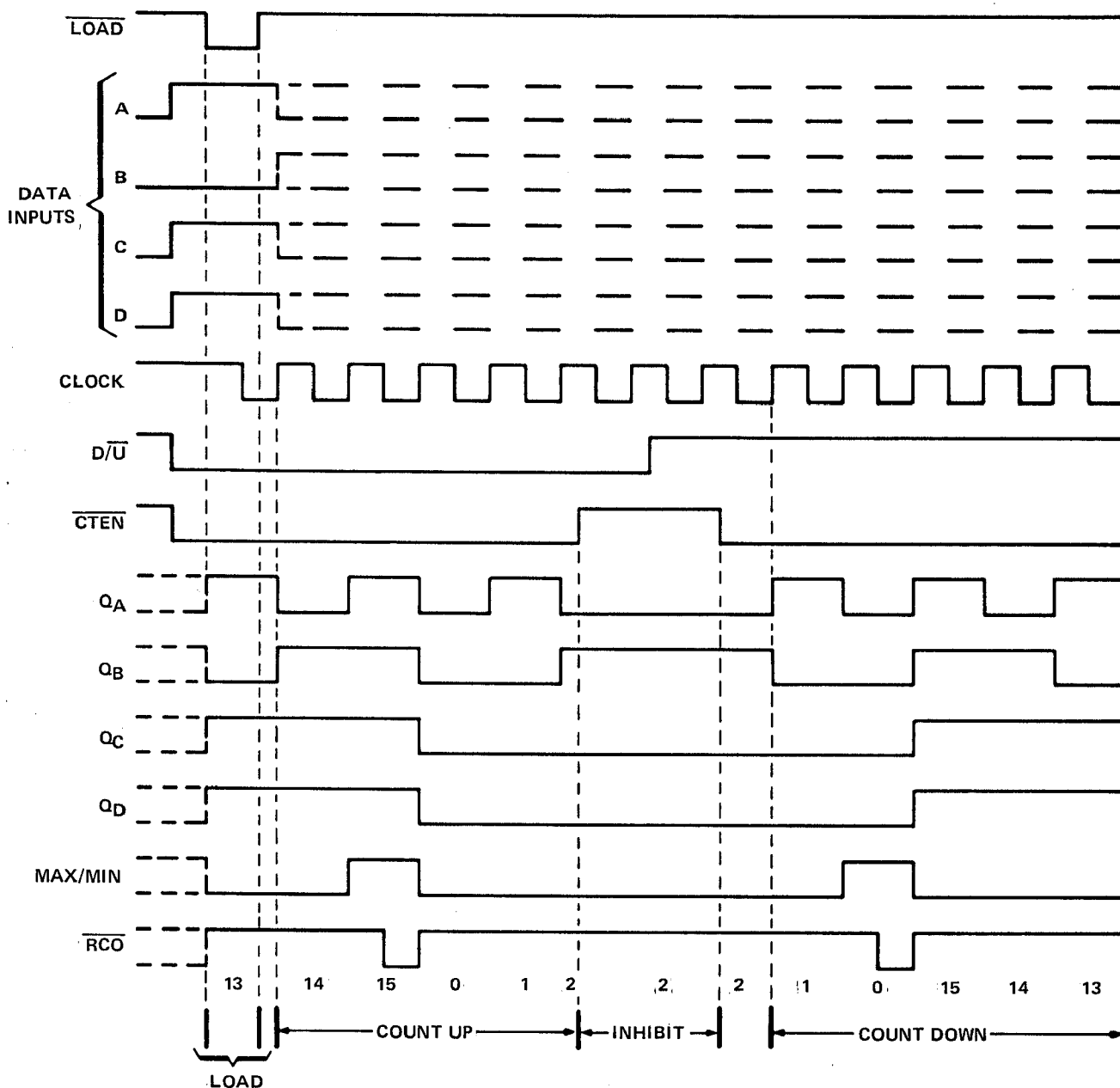
SDLS072 – DECEMBER 1972 – REVISED MARCH 1988

'191, 'LS191 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



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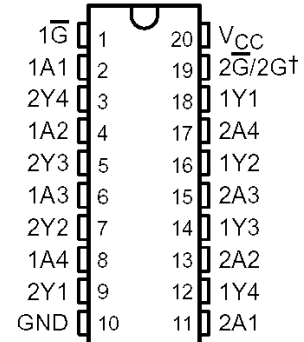
SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SDLS144B – APRIL 1985 – REVISED FEBRUARY 2002

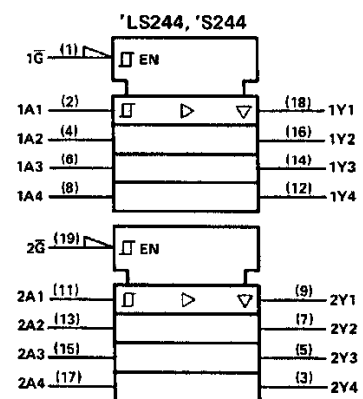
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- Hysteresis at Inputs Improves Noise Margins

description

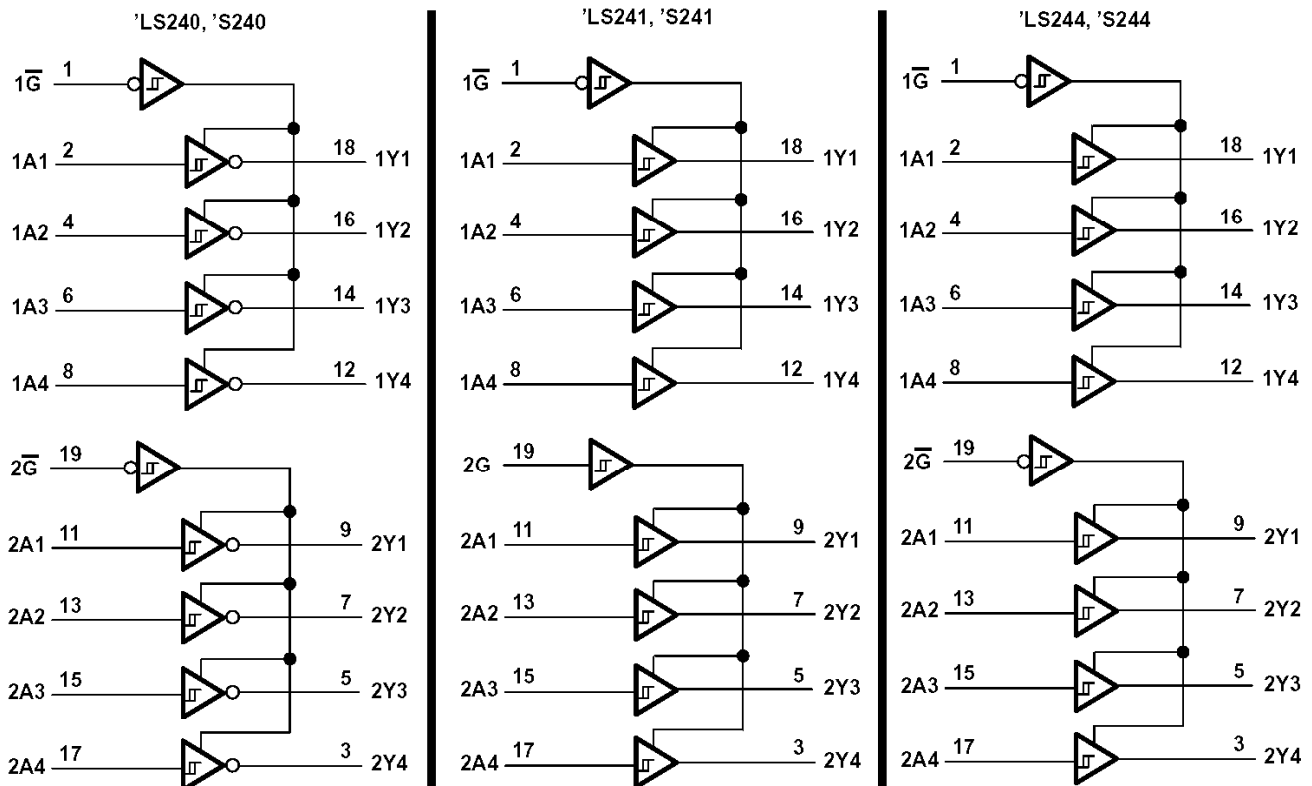
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical, active-low output-control (\overline{G}) inputs, and complementary output-control (G and \overline{G}) inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise margin. The SN74LS' and SN74S' devices can be used to drive terminated lines down to 133 Ω .



† 2G for 'LS241 and 'S241 or $2\overline{G}$ for all other drivers.



logic diagram (positive logic)



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

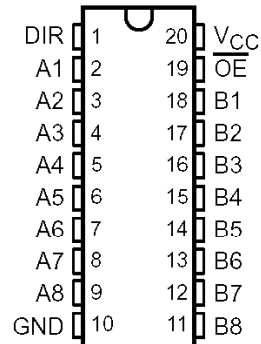
SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDLS146A – OCTOBER 1976 – REVISED FEBRUARY 2002

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce dc Loading on Bus Lines
- Hysteresis at Bus Inputs Improves Noise Margins
- Typical Propagation Delay Times Port to Port, 8 ns

| TYPE | I _{OL} (SINK CURRENT) | I _{OH} (SOURCE CURRENT) |
|-----------|--------------------------------------|--|
| SN54LS245 | 12 mA | –12 mA |
| SN74LS245 | 24 mA | –15 mA |

SN54LS245 . . . J OR W PACKAGE
SN74LS245 . . . DB, DW, N, OR NS PACKAGE
(TOP VIEW)



description

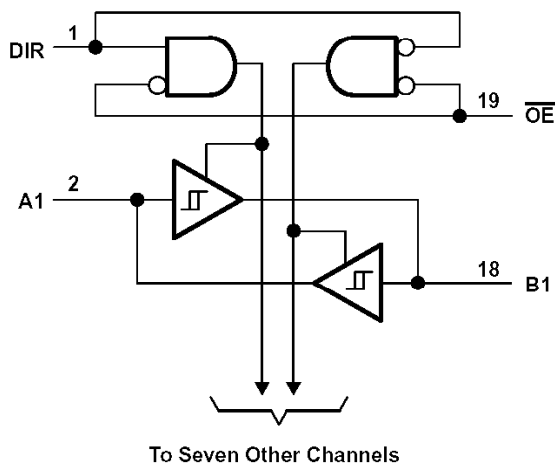
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can disable the device so that the buses are effectively isolated.

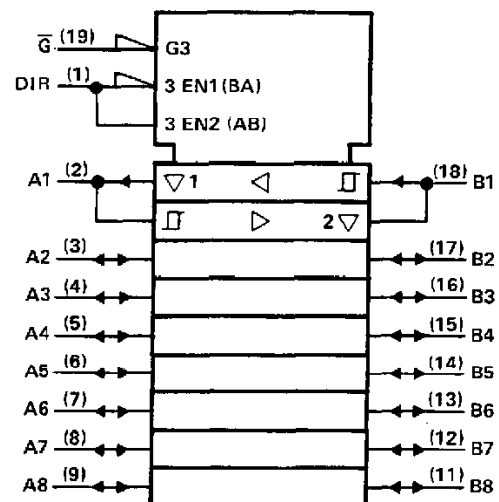
FUNCTION TABLE

| INPUTS | | OPERATION |
|--------|-----|-----------------|
| OE | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

logic diagram (positive logic)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.



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**SN54246, SN54247, SN54LS247, SN54LS248
SN74246, SN74247, SN74LS247, SN74LS248
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

MARCH 1974—REVISED MARCH 1988

'246, '247, 'LS247
feature

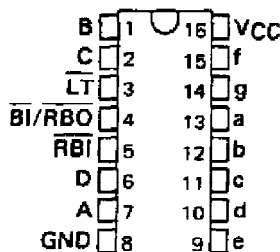
'LS248
feature

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- All Circuit Types Feature Lamp Intensity Modulation Capability

| TYPE | DRIVER OUTPUTS | | | | TYPICAL POWER DISSIPATION | PACKAGES |
|-----------|-----------------|-------------------------|-----------------|----------------|---------------------------------|----------|
| | ACTIVE LEVEL | OUTPUT CONFIGURATION | SINK CURRENT | MAX VOLTAGE | | |
| SN54246 | low | open-collector | 40 mA | 30 V | 320 mW | J,W |
| SN54247 | low | open-collector | 40 mA | 15 V | 320 mW | J,W |
| SN54LS247 | low | open-collector | 12 mA | 15 V | 35 mW | J,W |
| SN54LS248 | high | 2-k Ω pull-up | 2 mA | 5.5 V | 125 mW | J,W |
| SN74246 | low | open-collector | 40 mA | 30 V | 320 mW | J,N |
| SN74247 | low | open-collector | 40 mA | 15 V | 320 mW | J,N |
| SN74LS247 | low | open-collector | 24 mA | 15 V | 35 mW | J,N |
| SN74LS248 | high | 2-k Ω pull-up | 6 mA | 5.5 V | 125 mW | J,N |

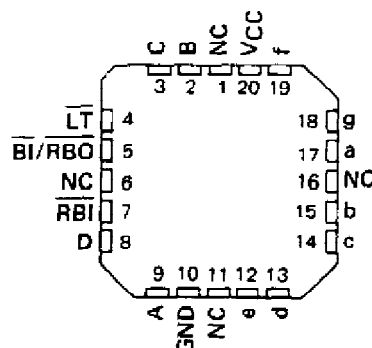
SN54246, SN54247 . . . J PACKAGE
SN54LS247 THRU SN54LS248 . . . J OR W PACKAGE
SN74246, SN74247 . . . N PACKAGE
SN74LS247, SN74LS248 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS247, SN54LS248 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection





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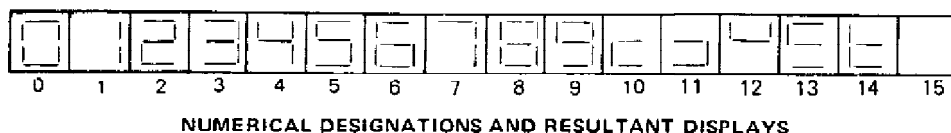
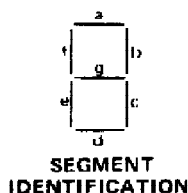
SN54246, SN54247, SN54LS247, SN54LS248 **SN74246, SN74247, SN74LS247, SN74LS248** **BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

description

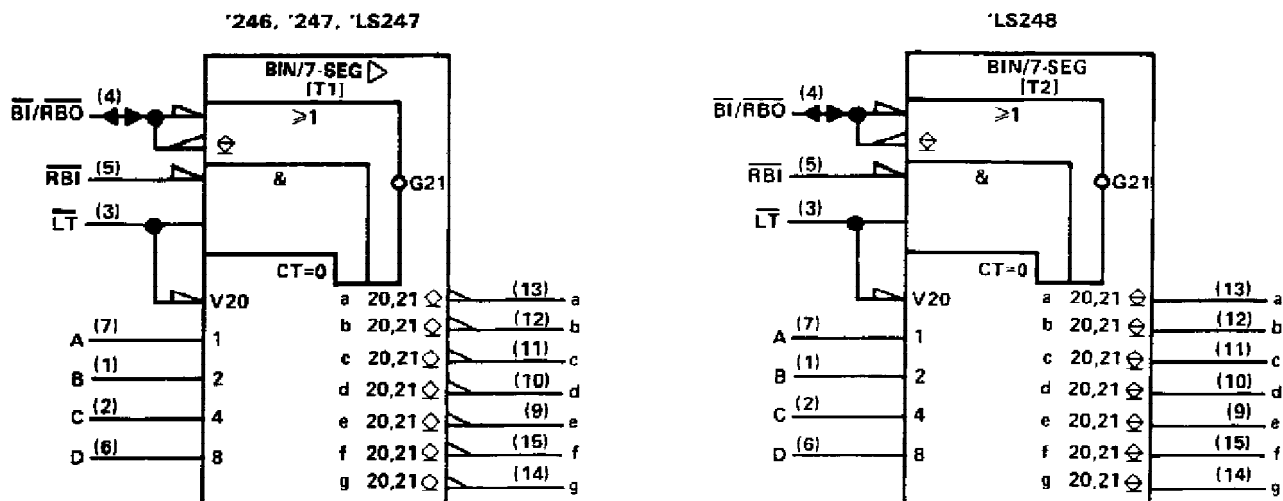
The '246 and '247 are electrically and functionally identical to the SN5446A/SN7446A, and SN5447A/SN7447A respectively, and have the same pin assignments as their equivalents. The 'LS247 and 'LS248 are electrically and functionally identical to the SN54LS47/SN74LS47 and SN54LS48/SN74LS48, respectively, and have the same pin assignments as their equivalents. They can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The '46A, '47A, 'LS47, and 'LS48 compose the  and the  without tails and the '246, '247, 'LS247, and 'LS248 compose the  and the  with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The '246, '247, and 'LS247 feature active-low outputs designed for driving indicators directly, and the 'LS248 features active-high outputs for driving lamp buffers. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

All of these circuits incorporate automatic leading and/or trailing-edge zero-blanking control ($\overline{\text{RBI}}$ and $\overline{\text{RBO}}$). Lamp test ($\overline{\text{LT}}$) of these types may be performed at any time when the $\overline{\text{BI/RBO}}$ node is at a high level. All types contain an overriding blanking input ($\overline{\text{BI}}$) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

Series 54 and Series 54LS devices are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74 and Series 74LS devices are characterized for operation from 0°C to 70°C .



logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

**SN54246, SN54247, SN54LS247, SN54LS248
SN74246, SN74247, SN74LS247, SN74LS248
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

'246, '247, 'LS247 FUNCTION TABLE (T1)

| DECIMAL OR FUNCTION | INPUTS | | | | | | $\overline{\text{BI}}/\text{RBO}^\dagger$ | OUTPUTS | | | | | | | NOTE |
|---------------------------|--------|-----|---|---|---|---|---|---------|-----|-----|-----|-----|-----|-----|------|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | ON | ON | ON | ON | ON | ON | OFF | 1 |
| 1 | H | X | L | L | L | H | H | OFF | ON | ON | OFF | OFF | OFF | OFF | |
| 2 | H | X | L | L | H | L | H | ON | ON | OFF | ON | ON | OFF | ON | |
| 3 | H | X | L | L | H | H | H | ON | ON | ON | ON | OFF | OFF | ON | |
| 4 | H | X | L | H | L | L | H | OFF | ON | ON | OFF | OFF | ON | ON | |
| 5 | H | X | L | H | L | H | H | ON | OFF | ON | ON | OFF | ON | ON | |
| 6 | H | X | L | H | H | L | H | ON | OFF | ON | ON | ON | ON | ON | |
| 7 | H | X | L | H | H | H | H | ON | ON | ON | OFF | OFF | OFF | OFF | |
| 8 | H | X | H | L | L | L | H | ON | ON | ON | ON | ON | ON | ON | |
| 9 | H | X | H | L | L | H | H | ON | ON | ON | ON | OFF | ON | ON | |
| 10 | H | X | H | L | H | L | H | OFF | OFF | OFF | ON | ON | OFF | ON | |
| 11 | H | X | H | L | H | H | H | OFF | OFF | ON | ON | OFF | OFF | ON | |
| 12 | H | X | H | H | L | L | H | OFF | ON | OFF | OFF | OFF | ON | ON | |
| 13 | H | X | H | H | L | H | H | ON | OFF | OFF | ON | OFF | ON | ON | |
| 14 | H | X | H | H | H | L | H | OFF | OFF | OFF | ON | ON | ON | ON | |
| 15 | H | X | H | H | H | H | H | OFF | OFF | OFF | OFF | OFF | OFF | OFF | |
| $\overline{\text{BI}}$ | X | X | X | X | X | X | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 2 |
| $\overline{\text{RBI}}$ | H | L | L | L | L | L | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 3 |
| $\overline{\text{LT}}$ | L | X | X | X | X | X | H | ON | ON | ON | ON | ON | ON | ON | 4 |

'LS248 FUNCTION TABLE (T2)

| DECIMAL OR FUNCTION | INPUTS | | | | | | $\overline{\text{BI}}/\text{RBO}^\dagger$ | OUTPUTS | | | | | | | NOTE |
|---------------------------|--------|-----|---|---|---|---|---|---------|---|---|---|---|---|---|------|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | H | H | H | H | H | H | L | 1 |
| 1 | H | X | L | L | L | H | H | L | H | H | L | L | L | L | |
| 2 | H | X | L | L | H | L | H | H | H | L | H | H | L | H | |
| 3 | H | X | L | L | H | H | H | H | H | H | H | L | L | H | |
| 4 | H | X | L | H | L | L | H | L | H | H | L | L | H | H | |
| 5 | H | X | L | H | L | H | H | H | L | H | H | L | H | H | |
| 6 | H | X | L | H | H | L | H | H | L | H | H | H | H | H | |
| 7 | H | X | L | H | H | H | H | H | H | H | L | L | L | L | |
| 8 | H | X | H | L | L | L | H | H | H | H | H | H | H | H | |
| 9 | H | X | H | L | L | H | H | H | H | H | H | L | H | H | |
| 10 | H | X | H | L | H | L | H | L | L | L | H | H | L | H | |
| 11 | H | X | H | L | H | H | H | L | L | H | H | L | L | H | |
| 12 | H | X | H | H | L | L | H | L | H | L | L | L | H | H | |
| 13 | H | X | H | H | L | H | H | H | L | L | L | H | L | H | |
| 14 | H | X | H | H | H | L | H | L | L | L | H | H | H | H | |
| 15 | H | X | H | H | H | H | H | L | L | L | L | L | L | L | |
| $\overline{\text{BI}}$ | X | X | X | X | X | X | L | L | L | L | L | L | L | L | 2 |
| $\overline{\text{RBI}}$ | H | L | L | L | L | L | L | L | L | L | L | L | L | L | 3 |
| $\overline{\text{LT}}$ | L | X | X | X | X | X | H | H | H | H | H | H | H | H | 4 |

H = high level, L = low level, X = irrelevant

- NOTES: 1. The blanking input ($\overline{\text{BI}}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{\text{RBI}}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input ($\overline{\text{BI}}$), all segment outputs are low regardless of the level of any other input.
3. When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output ($\overline{\text{BI}}/\text{RBO}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

$^\dagger \overline{\text{BI}}/\text{RBO}$ is wire-AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple-blanking output ($\overline{\text{RBO}}$).

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SN54HCT541, SN74HCT541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS306C - JANUARY 1996 - REVISED AUGUST 2003

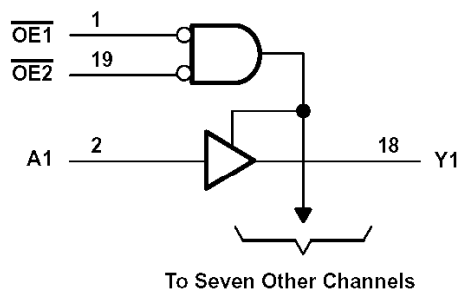
- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current 3-State Outputs Interface Directly With System Bus or Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 12$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)

description

These octal buffers and line drivers are designed to have the performance of the popular 'HC240 series devices and to offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed circuit board layout.

The 3-state control gate is a 2-input NOR. If either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state. The 'HCT541 devices provide true data at the outputs.

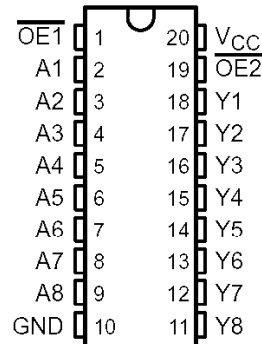
logic diagram (positive logic)



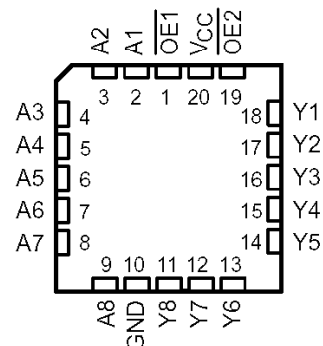
FUNCTION TABLE
(each buffer/driver)

| INPUTS | | | OUTPUT Y |
|------------------|------------------|---|-------------|
| $\overline{OE1}$ | $\overline{OE2}$ | A | |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

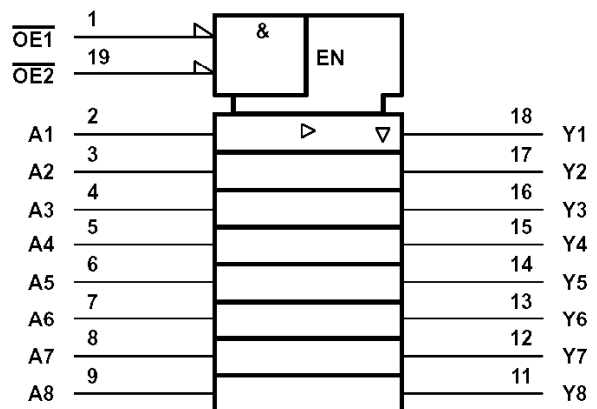
SN54HCT541 ... J OR W PACKAGE
SN74HCT541 ... DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCT541 ... FK PACKAGE
(TOP VIEW)



logic symbol†



† This symbol is in accordance with
ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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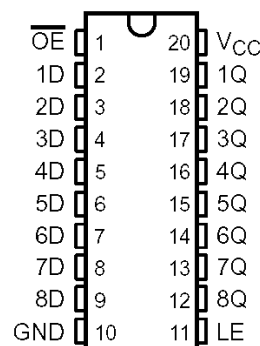
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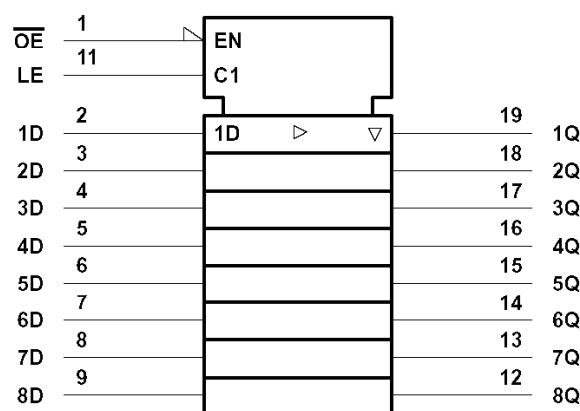
SCLS176E – MARCH 1984 – REVISED JULY 2003

- SN54HCT573 . . . J OR W PACKAGE
SN74HCT573 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



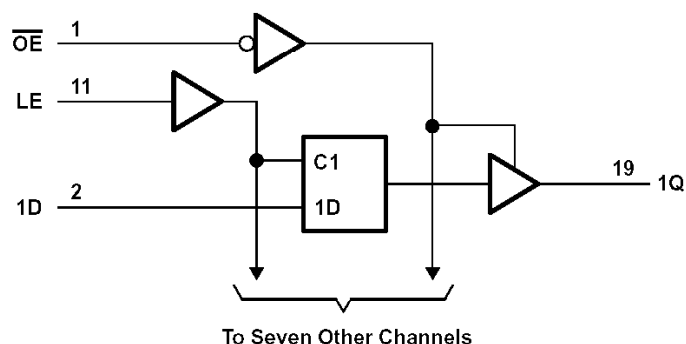
These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The 'HCT573 devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

logic symbol†



A buffered output-enable (\overline{OE}) input can be used to buffer the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

logic diagram (positive logic)



| INPUTS | | | OUTPUT Q |
|--------|----|---|----------------|
| OE | LE | D | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |



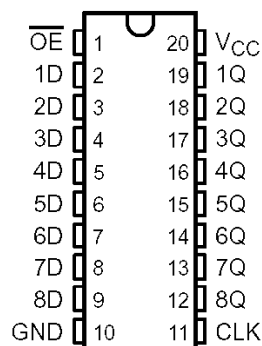
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SN54HCT574, SN74HCT574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS177E - MARCH 1984 - REVISED AUGUST 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current 3-State Noninverting Outputs Drive Bus Lines Directly or Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 22$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- Bus-Structured Pinout

SN54HCT574 ... J OR W PACKAGE
SN74HCT574 ... DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



description

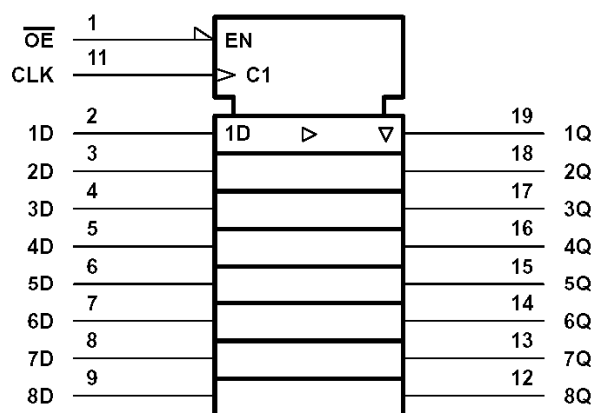
These octal edge-triggered D-type flip-flops feature 3-state outputs designed specifically for bus driving. The 'HCT574 devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

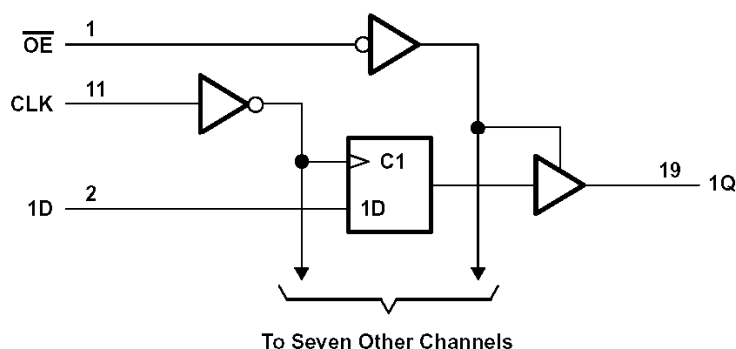
\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT Q |
|-----------------|------------|---|-------------|
| \overline{OE} | CLK | D | |
| L | \uparrow | H | H |
| L | \uparrow | L | L |
| L | H or L | X | Q_0 |
| H | X | X | Z |



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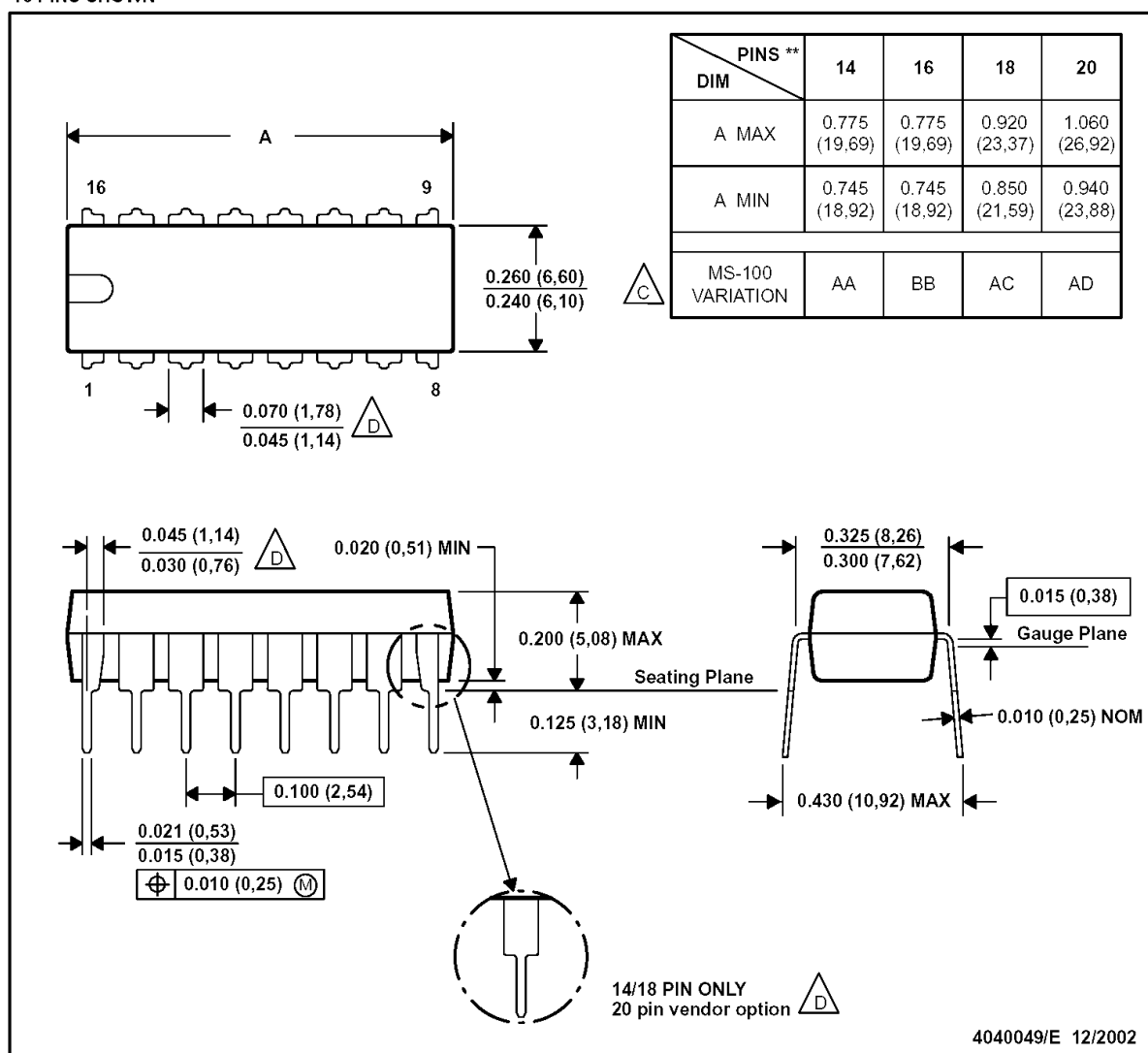
Ezekről a helyekről további részletes adatlapok tölthetők le.

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| National Semiconductor: | www.national.com |
| Motorola: | www.mot-sps.com |
| Philips: | www.semiconductors.philips.com |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.